HUAWEI LGA Module

PCM Audio Design Guide

Issue 04

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About This Document

Revision History

Document Version	Date	Chapter	Descriptions
01	2011-05-04		Creation
02	2015-02-10	2	Updated chapter 2 PCM Interface
		3	Deleted chapter 3 Timing in issue 01
		3	Updated chapter 3 Reference Design
		5	Deleted chapter 5 Audio Application of PCM in issue 01
03	2015-08-06	3.1	Deleted the description about TLV320AIC1106
		3.2.1	Deleted the chapter of TLV320AIC1106
04	2016-12-12	All	Deleted the description related to MU609

Scope

MU509 series

MC509 series

MU709 series

ME909u-521

Contents

1 Introduction

The purpose of this document is to describe some hardware specification which is useful to develop a product with Huawei LGA module supporting PCM (Pulse-Coded Modulation). This document is intended for customers who are integrators and about to implement their applications by using Huawei LGA module.

Huawei LGA module supports the PCM, which can be used for the module to transmit and receive digital audio data, and uses the PCM interface as part of the audio front end; therefore an external codec is easily allowed to be used instead of the internal codec. For example, through the PCM you could connect Huawei LGA module to a Bluetooth device.

Huawei LGA module has one PCM port. Please refer to the hardware guide of the module that you are in use to know the pin number of the PCM port.

2 PCM Interface

2.1 Definitions of Pins

Definitions of pins on the PCM interface of Huawei LGA module is as shown in Table 2-1 .

Table 2-1 Definitions of pins on the PCM interface

Pin No.	Pin Name		I/O	Description
	Normal	MUX		
5	PCM_SYNC	GPIO	I/O	PCM interface sync
6	PCM_DIN	GPIO	I	PCM I/F data in
7	PCM_DOUT	GPIO	O	PCM I/F data out
8	PCM_CLK	GPIO	I/O	PCM interface clock

NOTE

- When Huawei LGA module works on the master mode, PCM_CLK and PCM_SYNC pins are in the output status; when it works on the slave mode, PCM_CLK and PCM_SYNC pins are in the input status.
- Each module has two editions: Data only or Telematics. Data only does not support the PCM function.
- Following configurations in section 2.2 , except PCM data polarity, can be modified by **AT^CPCM** command.

2.2 Configuration Modes

2.2.1 PCM Working Mode

Huawei LGA module supports three PCM working modes, including MASTER_PRIM mode, MASTER_AUX mode and SLAVE mode.

PCM working mode	Description
MASTER_PRIM mode	In this mode, the PCM_CLK and PCM_SYNC signal clocks are generated by the module. And the frame format is short frame.
MASTER_AUX mode	In this mode, the PCM_CLK and PCM_SYNC signal clocks are generated by the module. And the frame format is long frame.
SLAVE mode	In this mode, the PCM_CLK and PCM_SYNC signal clocks are generated by the external CODEC chip.

Each module supports different PCM working modes, as shown in Table 2-2 .

Table 2-2 PCM working modes supported by different modules

Module	MASTER_PRIM mode	MASTER_AUX mode	SLAVE mode
MU509 series	Support (default)	Not support	Not support
MC509 series	Support (default)	Not support	Not support
MU709 series	Support (default)	Not support	Support
ME909u-521	Support (default)	Not support	Not support

2.2.2 PCM Data Format

Huawei LGA module supports three PCM data formats, including Linear, u-law and A-law. And each module supports different PCM data formats, as shown in Table 2-3 .

Table 2-3 PCM data formats supported by different modules

Module	Linear	u-law	A-law
MU509 series	Support (default)	Support	Not support
MC509 series	Support (default)	Support	Not support
MU709 series	Support (default)	Not support	Not support
ME909u-521	Support (default)	Not support	Not support

2.2.3 PCM Clock Signal

In MASTER_PRIM mode, the PCM bit clock supported by Huawei LGA module is 2.048 MHz only, except ME909u-521 also supports 4.096 MHz, as shown in Table 2-4 .

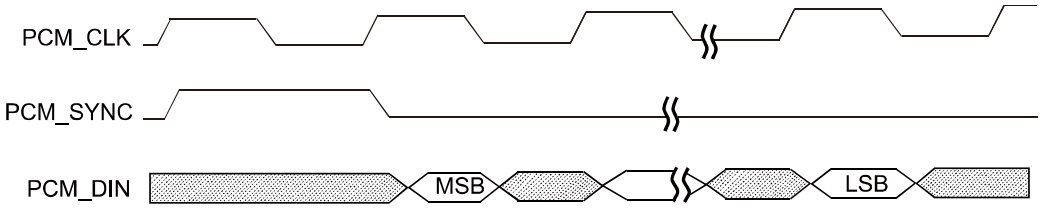
Table 2-4 PCM bit clocks supported by different modules in MASTER_PRIM mode

Module	2.048 Mhz	1.024 MHz	512 kHz	256 kHz	4.096 MHz
MU509 series	Support (default)	Not support	Not support	Not support	Not support
MC509 series	Support (default)	Not support	Not support	Not support	Not support
MU709 series	Support (default)	Not support	Not support	Not support	Not support
ME909u-521	Support (default)	Not support	Not support	Not support	Support

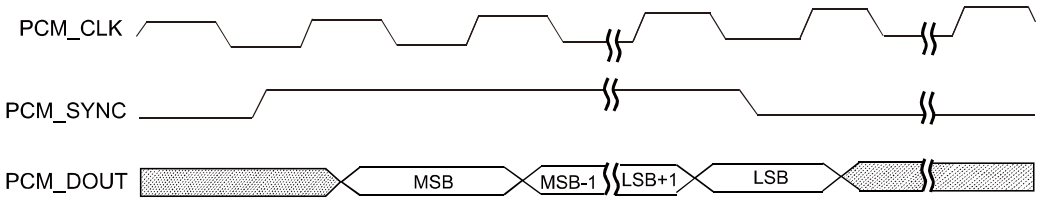
2.2.4 PCM SYNC Frame Format

PCM_SYNC supports long frame format and short frame format.

Short frame: PCM_SYNC only keeps one clock time high.



Long frame: PCM_SYNC keeps more than one clock time high.



NOTE

The two timing sequences above are not real, but used to describe the short and long frames.

Table 2-5 PCM SYNC frame formats supported by different modules

Module	Short frame	Long frame
MU509 series	Support (default)	Not support
MC509 series	Support (default)	Not support
MU709 series	Support (default)	Not support
ME909u-521	Support (default)	Not support

2.2.5 PCM Offset Setting

Huawei LGA module supports three PCM offset settings, including offset cleared, short sync offset set and long sync offset set.

PCM offset setting	Description
Offset cleared	The sync launched is aligned to the rising edge of the PCM_CLK.
Short sync offset set	The short sync sent to the external world in MASTER_PRIM mode is launched 1/4 cycle after the rising edge of the PCM_CLK.
Long sync offset set	The long sync sent to the external world in MASTER_AUX mode is launched 1/4 cycle ahead of the rising edge of PCM_CLK.

Table 2-6 PCM offset settings supported by different modules

Module	Offset cleared	Short sync offset set	Long sync offset set
MU509 series	Support (default)	Support	Not support
MC509 series	Support (default)	Support	Not support
MU709 series	Support (default)	Not support	Not support
ME909u-521	Support (default)	Not support	Not support

2.2.6 PCM DATA Polarity

Huawei LGA module supports two PCM data polarity settings, including falling edge and rising edge.

PCM data polarity	Description
Falling edge	The data input or output is followed the falling edge of PCM_CLK.
Rising edge	The data input or output is followed the rising edge of PCM_CLK.

Each module supports different PCM data polarity settings, as shown in Table 2-7 . And the setting cannot be modified by **AT^CPCM** command.

Table 2-7 PCM data polarity settings supported by different modules

Module	Falling edge	Rising edge
MU509 series	Support (default)	Not support

Module	Falling edge	Rising edge
MC509 series	Support (default)	Not support
MU709 series	Support (default)	Not support
ME909u-521	Support (default)	Not support

2.2.7 PCM DATA Length

The length of PCM data is 16 bits and cannot be changed.

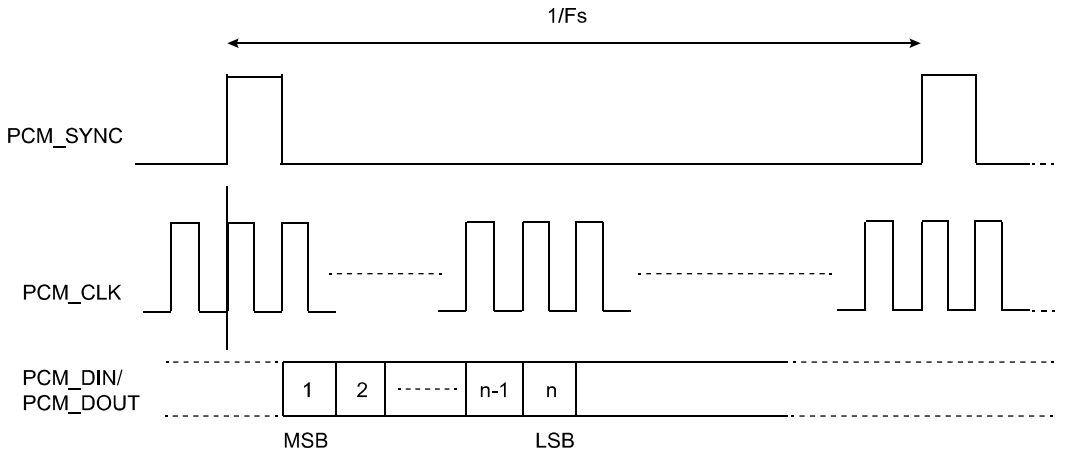
2.2.8 PCM SYNC Frequency

PCM SYNC frequency can be changed according to different PCM bit clocks.

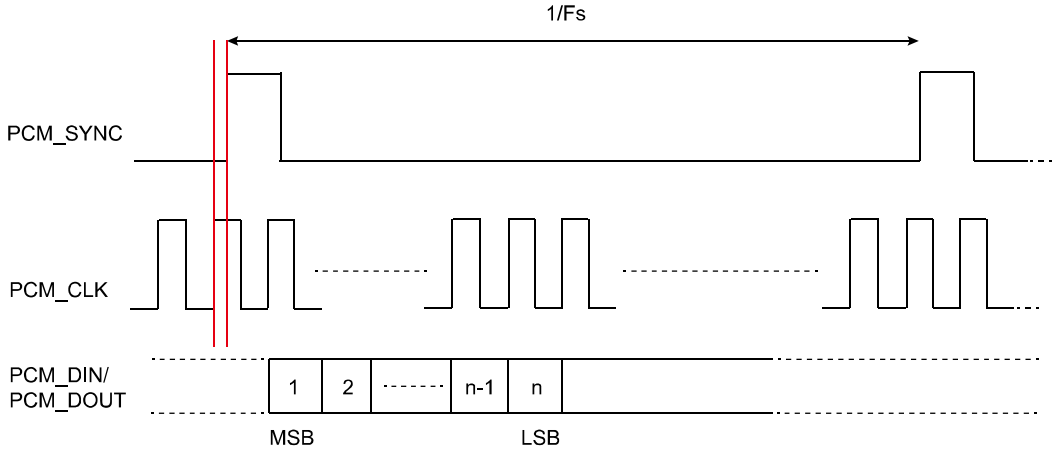
Bit clock / Sync	2.048 MHz	1.024 MHz	512 KHz	256 KHz	4.096 MHz
8K	√	×	×	×	×
16K	×	×	×	×	√

2.2.9 PCM Master Output Data Format

The default PCM master output data format is as shown in the following figure.



The data format of short sync offset set is as shown in the following figure. This mode is rarely used and only used for debugging to check the rising or fall timing.



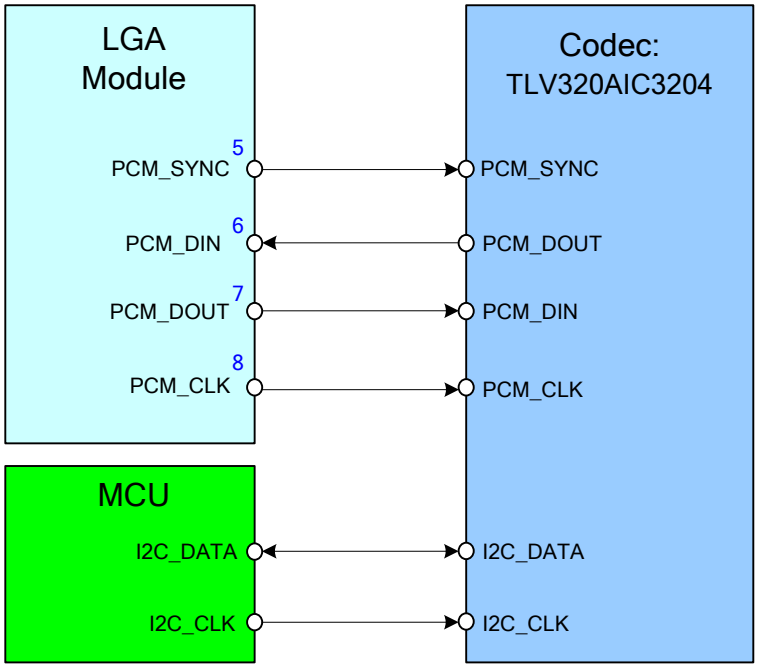
3 Reference Design

3.1 System Block

It is recommended that Huawei LGA module should work in PCM master mode. It means PCM_CLK and PCM_SYNC are generated by Huawei LGA module.

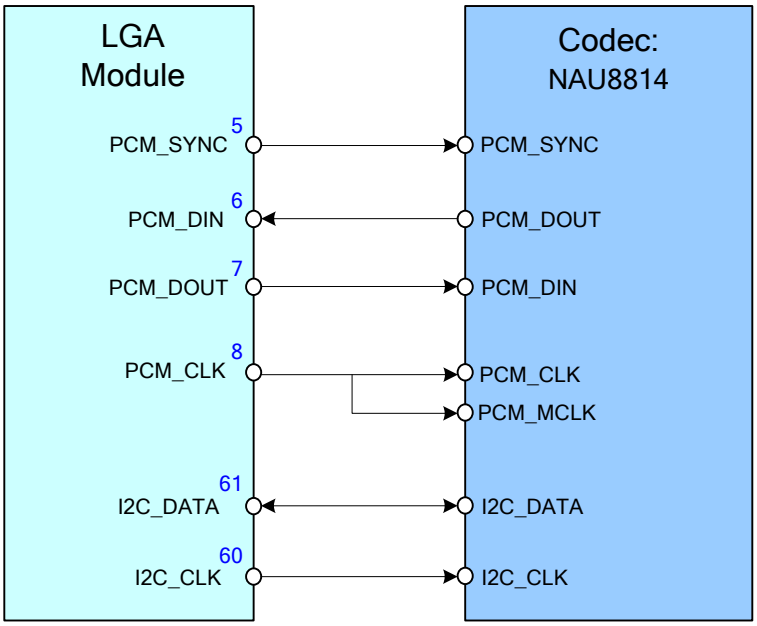
The codec of TLV320AIC3204 and NAU8814 are recommended to be used.

If customers have the I2C or SPI communication bus, TLV320AIC3204 or NAU8814 is recommended to be used. The recommended connections of TLV320AIC3204 are as shown in the following figure.



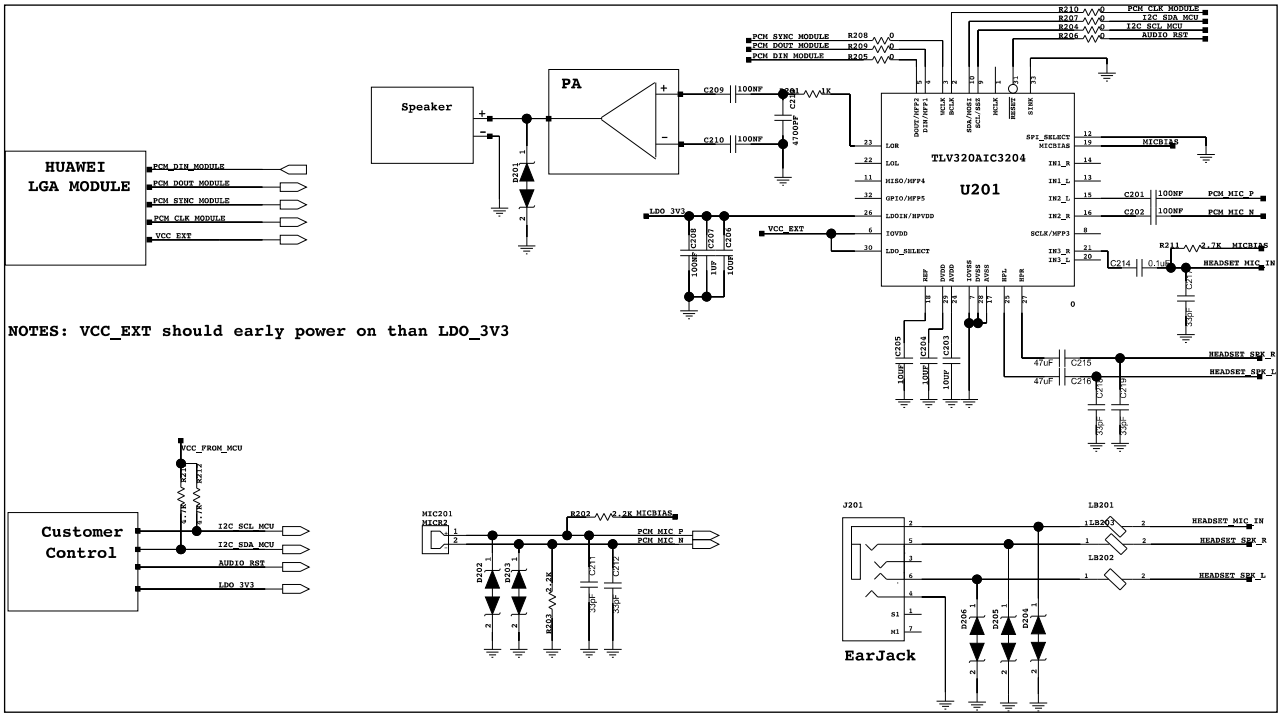
If customers have the communication bus and want to use NAU8814, the I2C of Huawei LGA module can be used. The module (MU709) can control NAU8814 by its I2C and does not need MCU anymore. In addition, Huawei LGA module provides **AT^CPCM** command to control NAU8814.

The recommended connections of NAU8814 are as shown in the following figure. This solution needs the support of Huawei LGA module's software. If customers want to use this function, you should connect us for more information.



3.2 Reference Schematic and Software Configuration

3.2.1 TLV320AIC3204



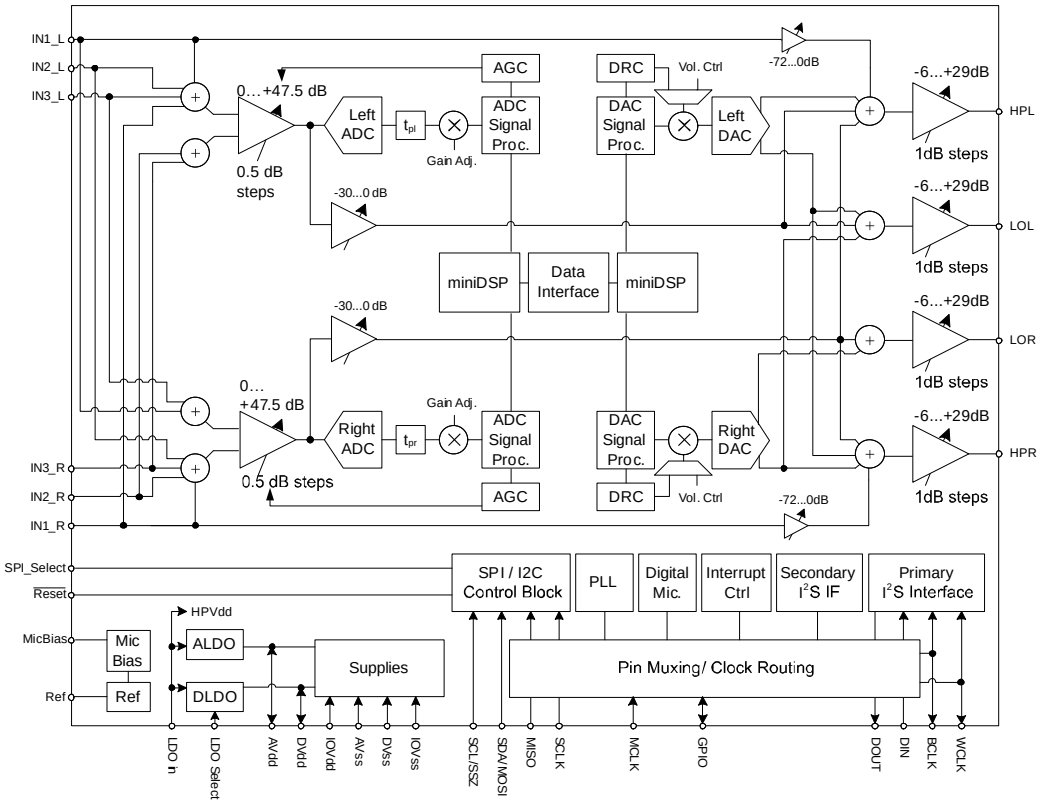
The referenced codec software configuration of TLV320AIC3204 is as follows.

NOTE

Values in gray color must not be changed, while values in green color can be changed.

```
static reg_addr_data aic3204_software_config[]=
{
    //Software Reset
    {0x00,0x00},
    {0x01,0x01},    //Reset Codec. You should wait more than 1ms during
this initialization phase.

    //Clock Setting  //If you use the follows Clock Setting, you do not
need crystal oscillator any more.
    //BCLK to PLL
    {0x00,0x00},
   {0x04,0x07},    // PLL Clock is CODEC_CLKIN   BCLK pin is input to PLL
    {0x05,0x91},    //Set PLL P and R value
    {0x06,0x28},    //Set PLL J value

    {0x0b,0x94},    //NDAC Divider Power Control
    {0x0c,0x81},    //MDAC Divider Power Control
    {0x0d,0x02},    //DAC OSR MSB Value Setting
   {0x0e,0x00},    //DAC OSR LSB Value Setting

    {0x12,0xA8},    //NADC Value Setting
    {0x13,0x82},    //MADC Value Setting

    //audio interface DSP mode
    //For Slave Mode
    {0x1B,0x40},    // We suggest customers use Slave Mode.
    {0x1C,0x01},

    //Signal Processing Settings
    {0x3C,0x01},    //Select PRB_P1 (Different Blocks means different
consumption and tone quality) PlayBack.
    {0x3D,0x01},    //Select PRB_R1 Record.

    //Configure Power Supplies
    {0x00,0x01},    //Select Register 1
    {0x01,0x08},    //Disabled weak connection of AVDD with DVDD
    {0x02,0xA1},    //LDO Configuration
    {0x47,0x32},    //Analog inputs power up time is 3.1 ms
   {0x7B,0x01},    // Reference will power up in 40ms when analog blocks
are powered up

    //uplink Setup
   {0x33,0x60},    // MICBIAS powered up;  10: MICBIAS = 2.075V(CM =
0.75V)  or MICBIAS = 2.5V(CM = 0.9V)
    {0x34,0x04},    // IN3L is routed to Left MICPGA with 10k resistance
//You can change value according to hardware design
    {0x36,0x40},    //IN3R is routed to Left MICPGA with 10k resistance
// You can change value according to hardware design
    {0x3B,0x35},   // Left MICPGA Volume Control  PGA=24dB
//programmable gain amplifiers (PGA)
    {0x3C,0x35},   // Right MICPGA Volume Control  PGA=24dB
```

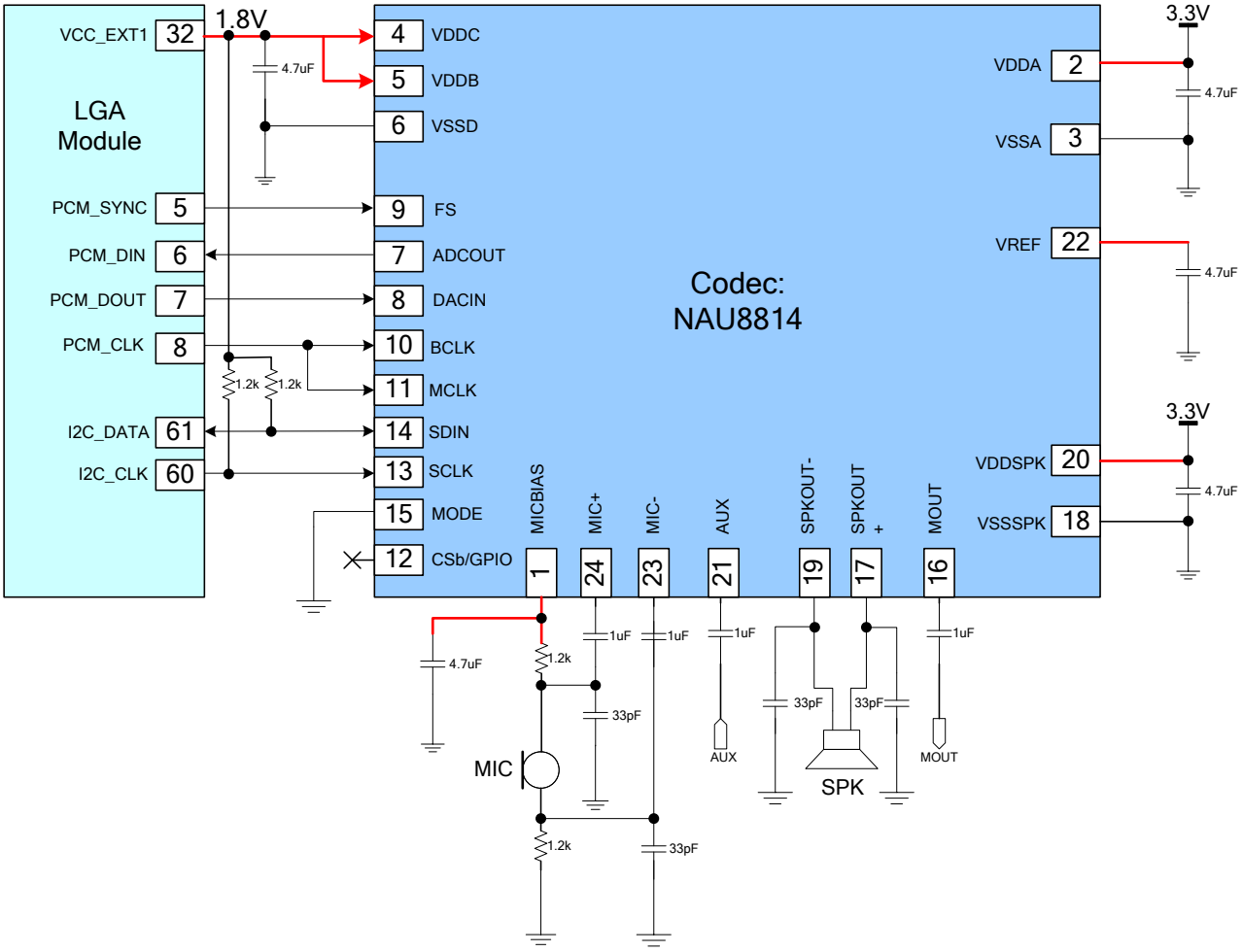
```
    {0x00,0x00},   //Select Register 0
    {0x51,0xC0},   //Left Channel ADC is powered up    Right Channel ADC
is powered up
   {0x52,0x00},   //Left ADC Channel Un-muted
   {0x53,0x00},   // Left ADC Channel Volume Control  ADC gain=0dB

   //Playback Setup

   {0x00,0x01},
    {0x09,0x3C},       //HPL、HPR、LOL、LOR is powered up
   {0x0C,0x08},      //Left Channel DAC reconstruction filter's positive
terminal is routed to HPL
                    //If you use LOR or LOL, you should change this value
   {0x0D,0x01},      //HPL output is routed to HPR (use when HPL and HPR
output is powered by AVDD)

    {0x10,0x00},      //HPL driver is not muted   HPL driver gain is 0dB
    {0x11,0x00},      // HPR driver is not muted   HPR driver gain is 0dB
    {0x12,0x00},       // LOL driver is not muted   LOL driver gain is
0dB
    {0x13,0x00},      // LOR driver is not muted   LOR driver gain is 0dB
   {0x14,0x35},      //1101: Headphone ramps power up slowly in 16.0
time constants ( do not use for Rchg=25K)
                    //01: Headphone ramps power up time is determined with
6k resistance
    //DAC configuration
    {0x00,0x00},
   {0x3F,0xD6},     //Left DAC Channel Powered Up       Right DAC Channel
Powered Up
                  //Left DAC data Left Channel Audio Interface Data
Right DAC data Right Channel Audio Interface Data
               //Soft-Stepping is disabled
    {0x40,0x00},     //Left DAC Channel not muted       Right DAC Channel
not muted

    {0x41,0x08},      //Left DAC Channel Digital Volume Control Setting
    {0x42,0x08},      //Right DAC Channel Digital Volume Control Setting
};
```



AT^CPCM is the AT command for the configuration of PCM. For the details, please refer to the module's AT command interface specification. If using the codec configuration above, you cannot change parameter values of **AT^CPCM**, but you can run **AT^CPCM=0,0,0,0,0** to set them to default values.

3.2.2 NAU8814

The referenced design of NAU8814 is as shown in the following figure. For details, please refer to NAU8814 official website.



The referenced codec software configuration of NAU8814 is as follows.

```
static REGISTER_SETTING_T sNA8814_CODEC_SETTING[]=
{
    {0x01,0x001d},
    {0x02,0x0015},
    {0x03,0x0065},
    {0x04,0x0118},
    {0x06,0x0000},
    {0x07,0x000A},
    {0x0E,0x01B8},
    {0x2d,0x00b0},
    {0x36,0x003f}
};
```

AT^CPCM is the AT command for the configuration of PCM. For the details, please refer to the module's AT command interface specification.

If using the codec configuration above, you need to keep parameter values of **AT^CPCM** as default values.

If you want to use the module’s I2C to control NAU8814, please run **AT^CODECPOW=1** firstly and then dial others.