HUAWEI 30 mm × 30 mm LGA Module

Hardware Migration Guide

Issue 04

Date 2014-10-11

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About This Document

Revision History

Document Version	Date	Chapter	Descriptions
01	2011-05-17		Creation
02	2013-10-11	All	Updated
03	2014-02-18	All	Updated the description related to LED pins
			Updated the description related to UART pins
			Updated the description related to PCM audio pins
		3.5	Updated antenna interface compatibility design
04	2014-10-11	All	Added the description related to MU709 and ME909u-523

Contents

1 Overview

This document describes interface differences among Huawei Land Grid Array (LGA) series modules of 30 mm × 30 mm (size). With this document, you can learn interface differences among the MU509 (including MU509-b, MU509-c and MU509-g), MC509 (including MC509 and MC509-a), MU609, ME909u (including ME909u-521 and ME909u-523), and MU709 (including MU709s-2 and MU709s-6) and precautions for compatibility design of the preceding modules.

1.1 Introduction to Huawei 30 mm × 30 mm LGA Modules

Table 1-1 Bands and Rates of Huawei 30 mm × 30 mm LGA modules

Product	Bands	Rate
MU509-b	WCDMA Band 1/8 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s
MU509-c	WCDMA Band 2/5 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s
MU509-g	WCDMA Band 1/5 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s

Product	Bands	Rate
MC509	CDMA–BC 0/1 GPS Standalone	CDMA 1xRTT: UL 153.6 kbit/s; DL 153.6 kbit/s CDMA 1x EV-DOrA: UL 1.8 Mbit/s; DL 3.1 Mbit/s
MC509-a	CDMA–BC 0 GPS Standalone	CDMA 1xRTT: UL 153.6 kbit/s; DL 153.6 kbit/s CDMA 1x EV-DOrA: UL 1.8 Mbit/s; DL 3.1 Mbit/s
MU609	WCDMA Band 1/2/5/8 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz GPS Standalone/A-GPS	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: UL 5.76 Mbit/s; DL 14.4 Mbit/s
ME909u-521	LTE Band 1/2/3/5/7/8/20 WCDMA Band1/2/5/8 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz GPS Standalone/A-GPS	LTE FDD: UL 50 Mbit/s @20M BW cat3; DL 100 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 43.2 Mbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s
ME909u-523	LTE Band 2/4/5/17 WCDMA Band 2/4/5 GPS Standalone/A-GPS	LTE FDD: UL 50 Mbit/s; @20M BW cat3; DL 100 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 43.2 Mbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s; WCDMA PS: UL 384 kbit/s; DL 384 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s
MU709s-6	WCDMA Band 1/2/5 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s
MU709s-2	WCDMA Band 1/8 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s

Table 1-2 Overview of Huawei 30 mm × 30 mm LGA modules

Product	Interface	Temperature	Dimension (mm)
MU509	1 x SIM 1 × 8 wire UART 1 × USB (Full Speed) 2 × Microphone in 1 × Handset out 1 × Speaker out 1 × PCM 8 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.57
MC509	1 x UIM 1 × 8 wire UART 1 × USB (Full Speed) 2 × Microphone in 1 × Handset out 1 × Speaker out 1 × PCM 7 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × W_DISABLE 3 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –30°C to +75°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.65

Product	Interface	Temperature	Dimension (mm)
MU609	1 x SIM 1 × 8 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM 5 × GPIO 1 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 3 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.27
ME909u	1 x SIM 2 × 4 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM[1] 5 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 3 × Antenna **2 x ADC is only for ME909u-523**	Normal operating temperature: –20°C to +70°C Extended operating temperature: –30°C to +75°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.35
MU709	1 x USIM 1 × 8 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM 5 × GPIO 1 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 2 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.27

NOTE
[1]: The firmware function is planning for ME909u.

Figure 1-1 Huawei 30 mm × 30 mm LGA module block level functional compatibility

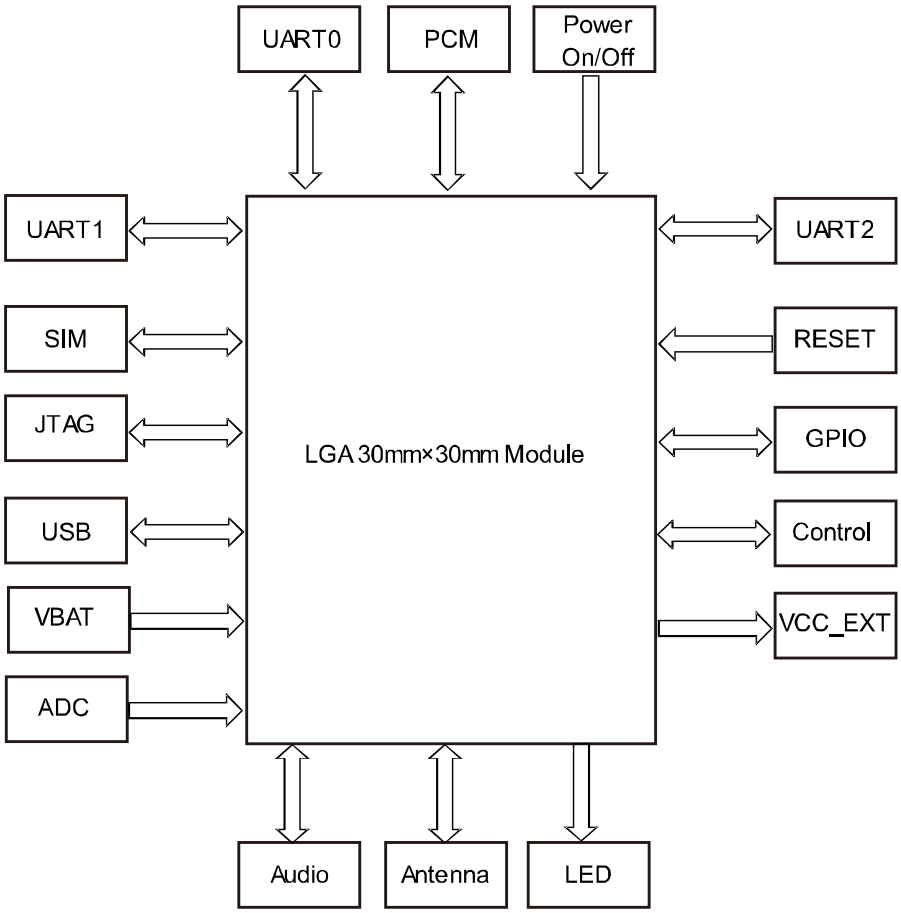


Table 1-3 Differences of LGA Interfaces

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
11	Control	WAKEUP_IN	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
71		WAKEUP_OUT	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
45		W_DISABLE (Now planning)	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
15		SLEEP_STATUS	Reserved (Planning for SLEEP_STATUS) CMOS 2.6 V	Reserved (Planning for SLEEP_STATUS) CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
81		POWER_ON_OFF	Y	Y	Y	Y	Y
100		RESIN_N	Y	Y	Y	Y	N
21–24		Tunable Antenna	N	N	N	CMOS 1.8 V (The firmware is being developed)	N
5–8	Audio	PCM audio	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	COMS 1.8 V (The firmware is being developed)	CMOS 1.8 V
38–41, 96–99		Analog audio	Y	Y	N	N	N
44	GPIO	GPIO	CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved
45			CMOS 2.6 V	W_DISABLE CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V
46			CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved
51, 55, 105, 109, 113			CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
107, 111, 115	Antenna	ANT pad size	1.5 mm × 1.0 mm	1.5 mm × 1.0 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
107, 111, 115		ANT function	Main (pin 107)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115)
31	VCC_EXT	VCC_EXT2 (2.6 V)	Y	Y	N	N	N
32		VCC_EXT1 (1.8 V)	Y	Y	Y	Y	Y
12, 13	VBAT	VBAT (3.3 V–4.2 V)	Five 220 μF capacitors needed	A 220 μF capacitors needed	Five 220 μF capacitors needed	Five 220 μF capacitors needed	Five 220 μF capacitors needed
30, 36, 42, 47, 72, 87, 93	JTAG	JTAG	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
14		PS_HOLD	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
100/47		RESIN_N/JTAG_SRST_N	RESIN_N (pin 100)	RESIN_N (pin 100)	RESIN_N (pin 100)	**JTAG_SRST_N (pin 47)** **JTAG reset for debugging**	N
73–80	UART	UART0	8-wire UART0 CMOS 2.6 V	8-wire UART0 CMOS 2.6 V	8-wire UART0 CMOS 1.8 V	4-wire UART0 CMOS 1.8V	8-wire UART0 CMOS 1.8 V
1–4		UART1	N	N	2-wire UART1 CMOS 1.8 V for debugging	4-wire UART1 CMOS 1.8V	2-wire UART1 CMOS 1.8 V for debugging
28, 29		UART2	N	N	N	2-wire UART1 CMOS 1.8 V only for debugging.	N
85, 86	USB	USB protocol	USB 2.0 Full Speed	USB 2.0 Full Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed
91	LED	LED_STATUS	Y	Y	Reserved (Planning for LED)	Reserved (Planning for LED)	Reserved (Planning for LED)

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
101		LED_MODE	Y	Y	Y	Y	Y
34	SIM/USIM/RUIM	USIM_VCC/RUIM_VCC	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V
88		USIM_RESET/RUIM_RESET	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V
89		USIM_DATA/RUIM_DATA	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V
90		USIM_CLK/RUIM_CLK	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V
102,104	ADC	ADC	N	N	N	0.3 V–VBATY[1]	N
49,53,57	GND	GND	GND	GND	GND	GND (ME909u-521) NOT USED (ME909u-523)	NOT USED

Note:
- N=not supported
- Y=supported
- You need to use a SIM/USIM card in MU509/MU609/ME909u and a RUIM card in MC509.
- The electrical features of CMOS 2.6 V interfaces refer to Table 1-4 .
- The electrical features of CMOS 1.8 V interfaces refer to Table 1-5 .
- [1]: The ME909u-523 module provides two ADC interfaces. ME909u-521 does not support ADC interface at present (The firmware is being developed).

Table 1-4 Electrical features of CMOS 2.6 V interfaces

Parameter	Description	Minimum Value	Maximum Value	Unit
V_{IH}	High-level input voltage	1.7	2.9	V
V_{IL}	Low-level input voltage	–0.3	0.9	V

Table 1-5 Electrical features of CMOS 1.8 V interfaces

Parameter	Description	Minimum Value	Maximum Value	Unit
V_{IH}	High-level input voltage	1.2	2.1	V

Parameter	Description	Minimum Value	Maximum Value	Unit
V_{IL}	Low-level input voltage	–0.3	0.6	V

NOTE

V_{IL} indicates Low-level Input voltage; V_{IH} indicates High-level Input voltage.

2 LGA Interface Differences

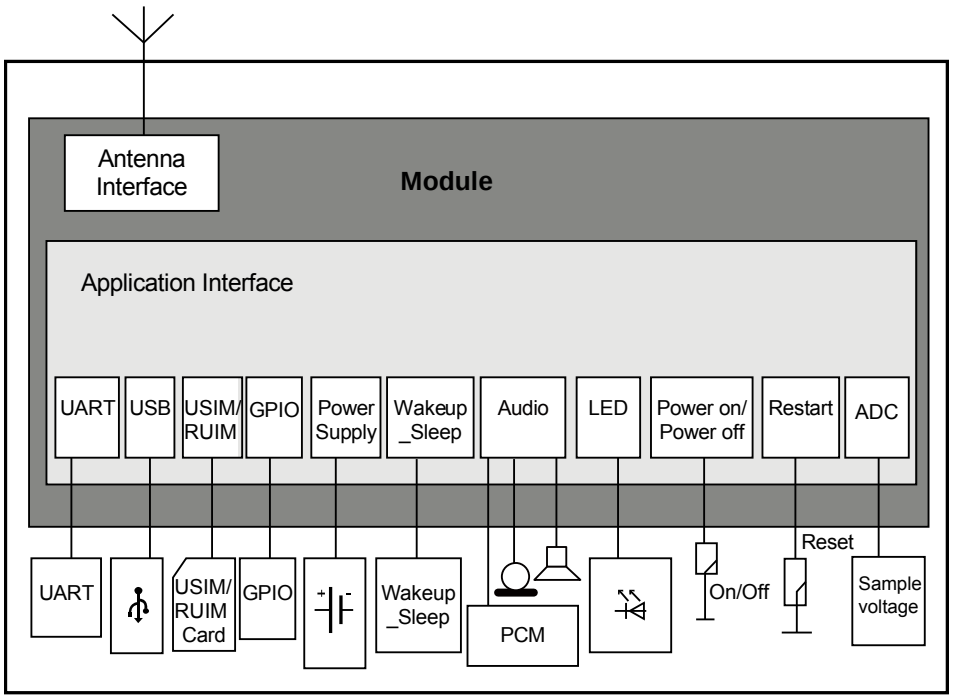
2.1 LGA Interfaces

2.1.1 Schematic Diagram of Interfaces

Huawei 30 mm × 30 mm LGA module provides 145 pads, on which pin 1 to pin 116 are defined as signal pins and pin 121 to pin 145 are defined as heat-dissipation ground pads.

Huawei 30 mm × 30 mm LGA module provides interfaces including power supply, antenna, Universal Serial Bus (USB), Universal Subscriber Identity Module (USIM)/Removable User Identity Module (RUIM), Universal Asynchronous Receiver-Transmitter (UART), audio, Pulse-code Modulation (PCM), Light-emitting Diode (LED), General-purpose I/O (GPIO), WAKEUP_IN, WAKEUP_OUT, SLEEP_STATUS, power on/power off, reset, Joint Test Action Group (JTAG) interfaces, ADC interface and so on.

Figure 2-1 Application block diagram of the 30 mm × 30 mm LGA module



2.2 Control Interface Compatibility Design

2.2.1 Detailed Interface Differences

Table 2-1 Differences of the Control interfaces

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
11	Control	WAKEUP_IN	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
71		WAKEUP_OUT	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
45		W_DISABLE (Now planning)	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V
15		SLEEP_STATUS	Reserved (Planning for SLEEP_STATUS) CMOS 2.6 V	Reserved (Planning for SLEEP_STATUS) CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
81		POWER_ON_OFF	Y	Y	Y	Y	Y
100		RESIN_N	Y	Y	Y	Y	N
21–24		Tunable Antenna	N	N	N	CMOS 1.8 V (The firmware is being developed.)	N

2.2.2 Control Interface Design Guide

WAKEUP_IN

The host can control LGA module to enter the sleep state through the WAKEUP_IN pin.

When WAKEUP_IN pin is in high level, the module is in the wakeup state.

When WAKEUP_IN pin is in low level, MU509/MC509 will be forced into sleep state; MU609/ME909u/MU709 will not be forced but be allowed into sleep state instead.

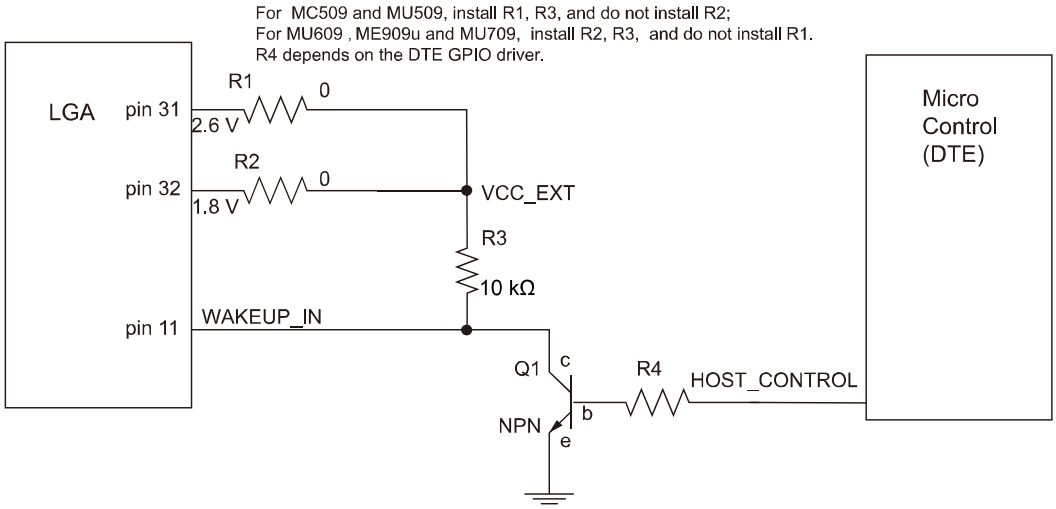
If WAKEUP_IN pin is floated, MU509/MC509 will keep high level internally, while MU609/ME909u/MU709 will keep low level internally.

For ME909u, WAKEUP_IN pin must be connected if you want to normally use the High-Speed UART in the future.

Table 2-2 Differences of WAKEUP_IN interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
11	Control	WAKEUP_IN	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V

Figure 2-2 The recommended connection of WAKEUP_IN pin



NOTE
R4 depends on the actual DTE requirements.

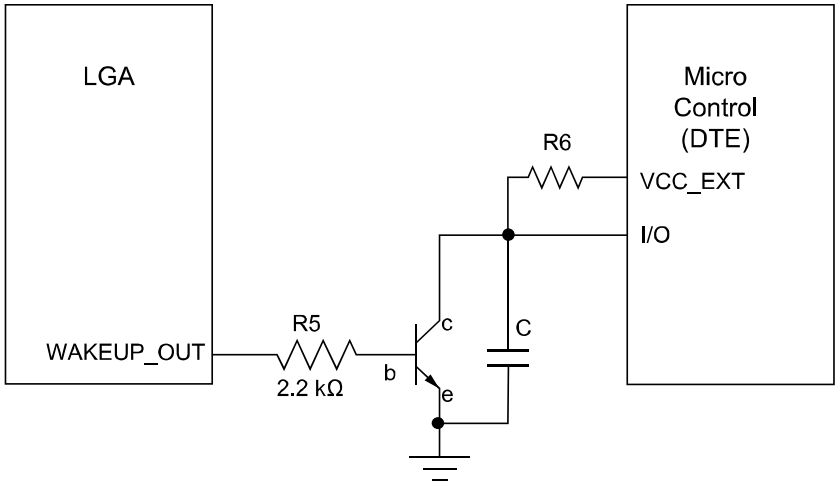
WAKEUP_OUT

The LGA module can wake up the host through the WAKEUP_OUT. To implement compatibility of the signal level, it is recommended that you connect the pin based on the circuit diagram shown in Figure 2-3 .

Table 2-3 Differences of WAKEUP_ OUT interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
71	Control	WAKEUP_OUT	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V

Figure 2-3 The recommended connection of the WAKEUP_OUT pin



NOTE

R6 depends on the actual DTE requirements.

SLEEP_STATUS

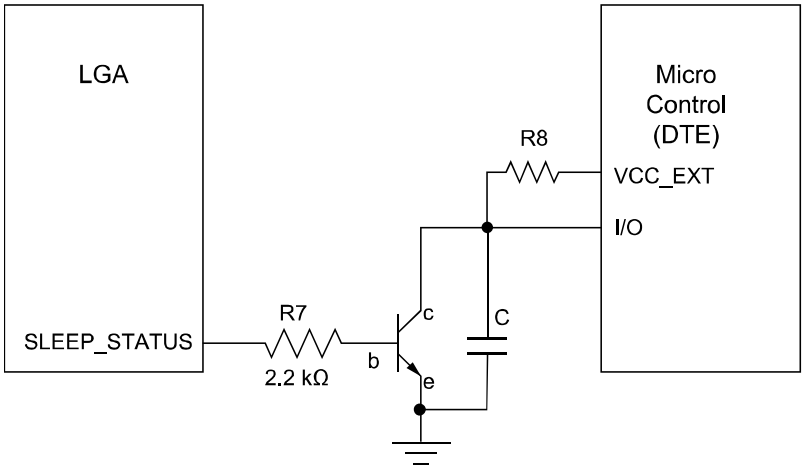
SLEEP_STATUS signal is used to indicate the sleep status of 30 mm × 30 mm LGA Module. The external devices can get to know whether the module is in sleep mode by reading SLEEP_STATUS pin.

When SLEEP_STATUS pin is in high level, 30 mm × 30 mm LGA modules are in wakeup state.

When SLEEP_STATUS pin is in low level, 30 mm × 30 mm LGA modules are in sleep state.

Figure 2-4 shows recommended circuit of the SLEEP_STATUS pin.

Figure 2-4 The recommended connection of the SLEEP_STATUS pin



NOTE
R8 depends on the actual DTE requirements.

W_DISABLE

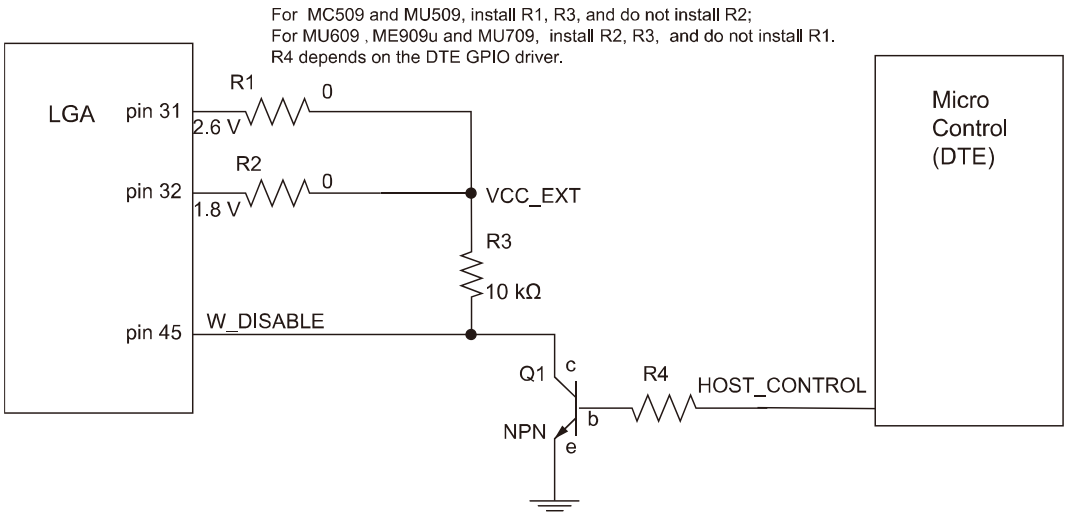
Pin 45 works as the W_DISABLE signal. The MC509 supports this function. MU609, MU709 and ME909u are now planning this pin (Pin 45) for W_DISABLE signal, while this pin for MU509 is GPIO.

This signal requires an external pull-up resistor, which should be pulled up to VCC_EXT1 (Pin 32) or VCC_EXT2 (Pin 31). The signal level differs between 30mm × 30mm LGA modules. Therefore, the MC509 uses pin 31 to provide the pull-up power supply and the MU609/ME909u/MU709 uses pin 32 to provide the pull-up power supply. The reference circuit diagram is shown in the following figure. A transistor is required to separate this signal from the host control signal.

Table 2-4 Differences of W_DISABLE interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
45	Control	W_DISABLE	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V		

Figure 2-5 The recommended connection of the W_DISABLE pin



POWER_ON_OFF

Pin 81 works as the POWER_ON_OFF signal. The diagram of recommended circuit is shown in Table 2-6 .

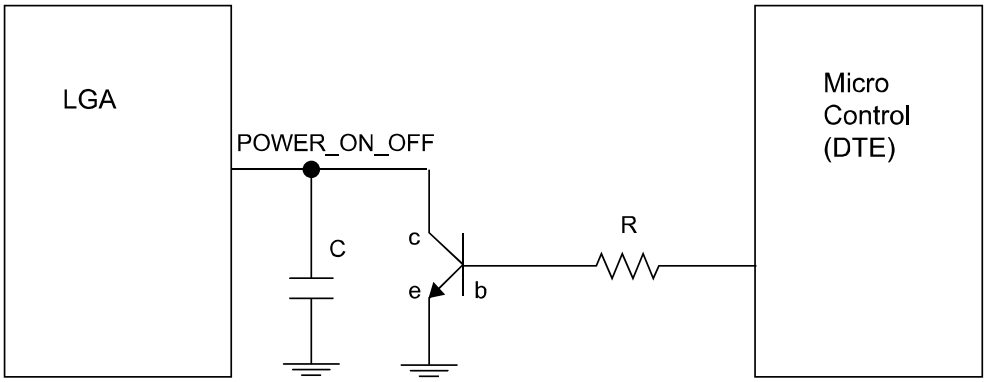
Table 2-5 Two states of POWER_ON_OFF interface

Item	Pin state	Description
1	Low (when Huawei 30 mm × 30 mm LGA module is in power off state.)	Huawei 30 mm × 30 mm LGA module is powered on. **POWER_ON_OFF pin should be pulled down for 0.5s to 1.0s.（At least 1s for MU709）**
2	Low (when Huawei 30 mm × 30 mm LGA module is in power on state.)	Huawei 30mm × 30mm LGA module is powered off. **POWER_ON_OFF pin should be pulled down for 3.5s to 4.0s.（At least 4s for MU709）**

Table 2-6 Differences of POWER_ON_OFF interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
81	Control	POWER_ON_OFF	Y	Y	Y	Y	Y

Figure 2-6 The recommended connection of the POWER_ON_OFF pin



RESIN_N

The MU709 module does not support the analogue RESIN_N interface.

Table 2-7 Differences of RESIN_N interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
100	Control	RESIN_N	Y	Y	Y	Y	N

The RESIN_N pin is used to reset the module's system. If the software of module stops responding, you can reset the hardware through the RESIN_N signal as shown

in Figure 2-8 . When a low-level pulse is supplied through the RESIN_N pin, the hardware will be reset. After the hardware is reset, the software starts powering on the module and reports relevant information according to the actual settings.

Figure 2-7 The recommended connection of the RESIN_N pin

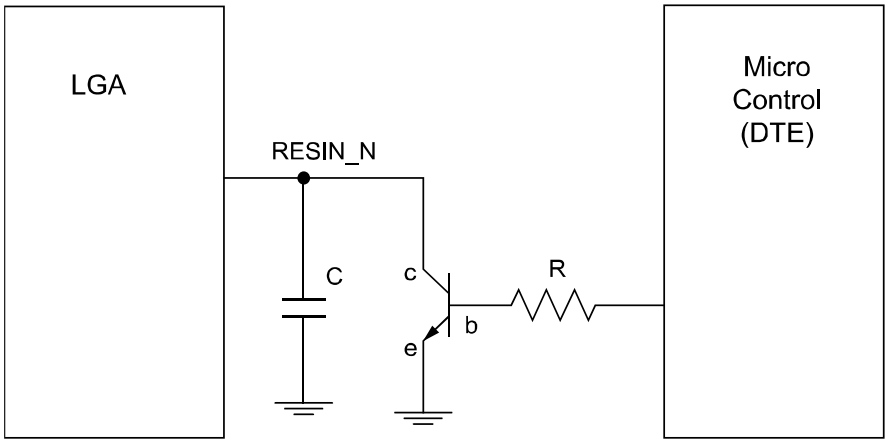
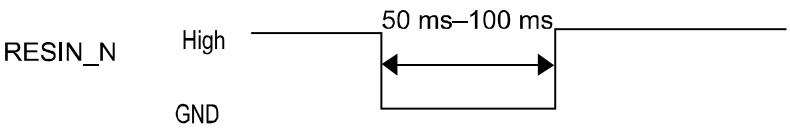


Figure 2-8 Reset pulse timing



NOTE
The RESIN_N pin must not be pulled down for more than 1s.

Tunable Antenna Control

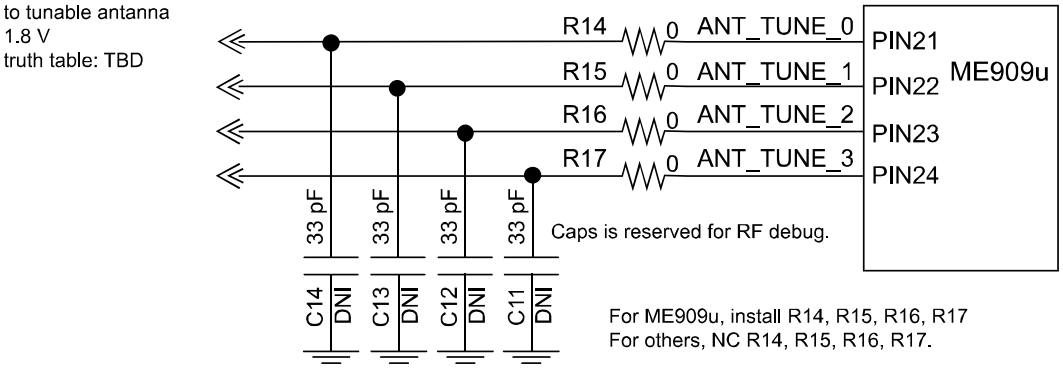
ME909u provides 4 tunable antenna control pins. The firmware with this feature is being developed.

Table 2-8 Differences of tunable antenna control pins

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
21	Control	ANT_TUNE0	N	N	N	CMOS 1.8 V	N
22		ANT_TUNE1	N	N	N	CMOS 1.8 V	N
23		ANT_TUNE2	N	N	N	CMOS 1.8 V	N
24		ANT_TUNE3	N	N	N	CMOS 1.8 V	N

The mapping of each band to ANT_TUNE outputs is configurable.

Figure 2-9 The circuit diagram of tunable antenna control



2.3 Audio Interface Compatibility Design

2.3.1 Detailed Interface Differences

For PCM Audio, MU509, MC509, MU609, ME909u and MU709 differ on the level.

For Analog Audio, MU509 and MC509 support Analog Audio, while MU609, ME909u and MU709 do not support Analog Audio.

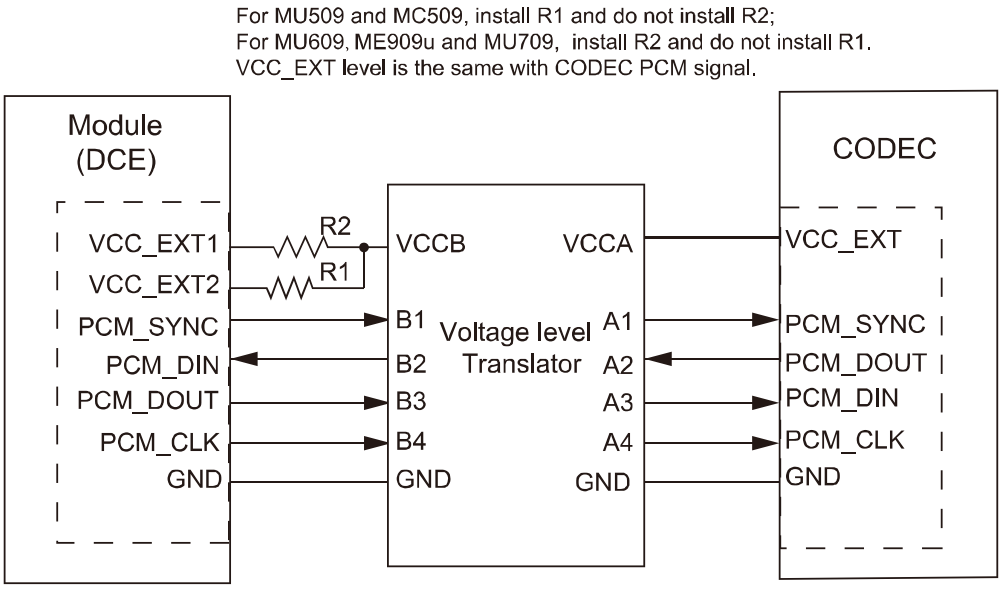
Table 2-9 Differences of the audio interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
5	PCM Audio	PCM_SYNC	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	COMS 1.8 V (The firmware is being developed)	CMOS 1.8 V
6		PCM_DIN	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V		CMOS 1.8 V
7		PCM_DOUT	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V		CMOS 1.8 V
8		PCM_CLK	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V		CMOS 1.8 V
38	Analog Audio	MIC2_P	Y	Y	N	N	N
39		MIC2_N	Y	Y	N	N	N
40		MIC1_P	Y	Y	N	N	N
41		MIC1_N	Y	Y	N	N	N
96		EAR_OUT_N	Y	Y	N	N	N
97		EAR_OUT_P	Y	Y	N	N	N
98		SPKR_OUT_P	Y	Y	N	N	N
99		SPKR_OUT_N	Y	Y	N	N	N

2.3.2 PCM Interface Design Guide

Please note that the different signal level of PCM between MU509/MC509 and MU609/ME909u/MU709. The signal of MU509 and MC509 is CMOS 2.6 V and MU609, MU709 and ME909u are CMOS 1.8 V. Therefore, you must consider compatibility during circuit designing.

Figure 2-10 The recommended connection of the PCM interface in the LGA module



NOTE

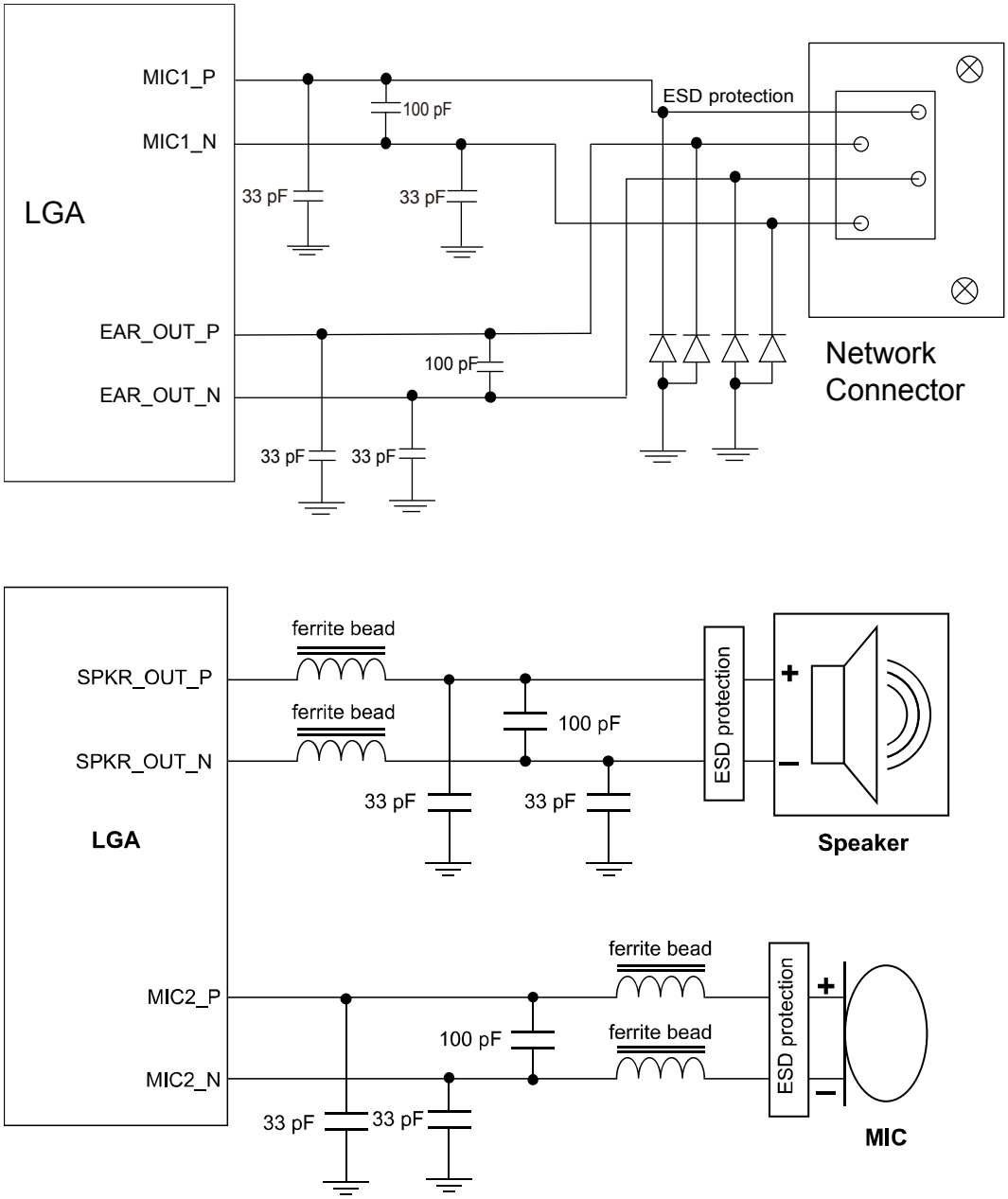
- The PCM function of ME909u is under development.
- PCM_SYNC: Output when PCM is in master mode;
- PCM_CLK: Output when PCM is in master mode;
- The PCM function of 30 mm × 30 mm LGA module is only supported in master mode until now.
- It is recommended that a TVS be used on the related interface, to prevent electrostatic discharge and protect integrated circuit (IC) components.

2.3.3 Audio Interface Design Guide

The MU609, MU709 and ME909u module do not support the analogue audio interface.

MU509 and MC509 module support two channels MIC: one channel EAR and one channel SPEAKER.

Figure 2-11 The circuit diagram of audio interface



2.4 GPIO Interface Compatibility Design

2.4.1 Detailed Interface Differences

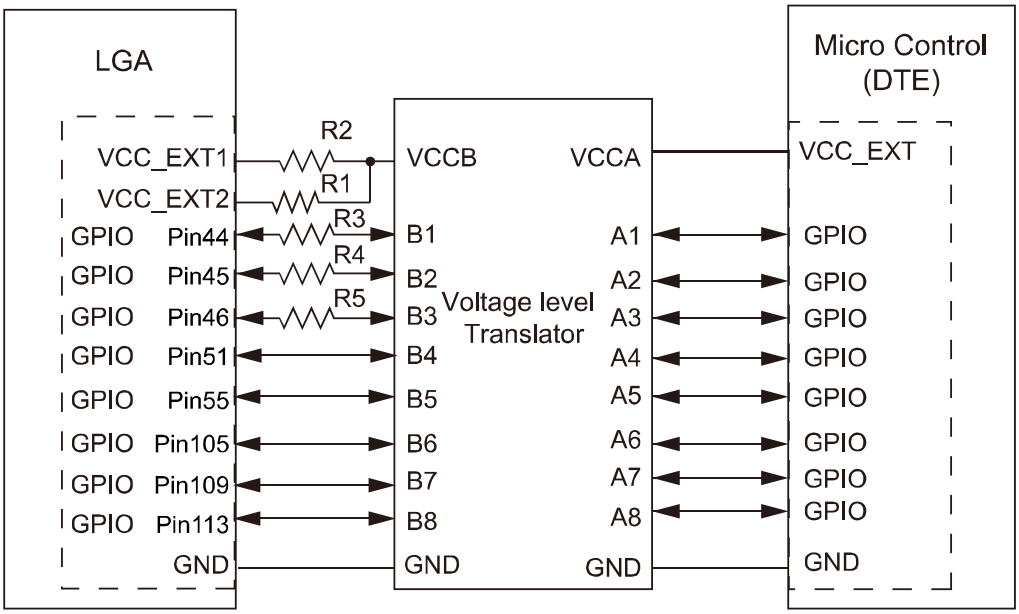
Please note the different signal level of GPIO between MU509/MC509 and MU609/ME909u/MU709. The signal of MU509 and MC509 are CMOS 2.6 V and MU609, MU709 and ME909u are CMOS 1.8 V. Therefore, you must consider the compatibility during circuit designing.

Table 2-10 Differences of the GPIO interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
44	GPIO	GPIO	CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved
45		GPIO	CMOS 2.6 V	W_DISABLE CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V
46		GPIO	CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved
51		GPIO	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
55		GPIO	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
105		GPIO	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
109		GPIO	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
113		GPIO	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V

Figure 2-12 The recommended connection of the GPIO pin

For MU509, install R1,R3,R4,R5 and do not install R2;
For MC509, please install R1,R3,R5, and donot install R2 and R4, design pin 45 referring to the design of W_DISABLE;
For MU609, ME909u and MU709, install R2 and do not install R1,R3,R4,R5.
VCC_EXT level is the same with DTE GPIO signal.
if MU509 does not need 8 GPIOs, please design pin 45 referring to the design of W_DISABLE in order to be compatible with MC509, MU609, MU709 and ME909u.



NOTE
The pin 45 of the MU609, MU709 and ME909u are planning for W_DISABLE.

2.5 Antenna Interface Compatibility Design

2.5.1 Detailed Interface Differences

Please note that the difference of antenna among 30 mm × 30 mm LGA modules. MU509 only supports MAIN_ANT. MC509, MU609 and ME909u support MAIN_ANT, AUX_ANT (Diversity) and GPS_ANT. MU709 supports MAIN_ANT and AUX_ANT (Diversity).

Table 2-11 Differences of the antenna interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
107	Antenna	MAIN_ANT	Y	Y	Y	Y	Y
111		GPS_ANT	N	Y	Y	Y	N
115		AUX_ANT	N	Y	Y	Y	Y

2.5.2 Antenna Interface Design Guide

To implement compatibility among the Huawei 30 mm × 30 mm LGA modules, pay attention to antenna interfaces pin 107 (MAIN_ANT), pin 111 (AUX_ANT), and pin 115 (GPS_ANT).

Pay attention to the interface differences among the MU509 and other 30 mm × 30 mm LGA modules.

Table 2-12 Differences of the antenna interface in pad size and function

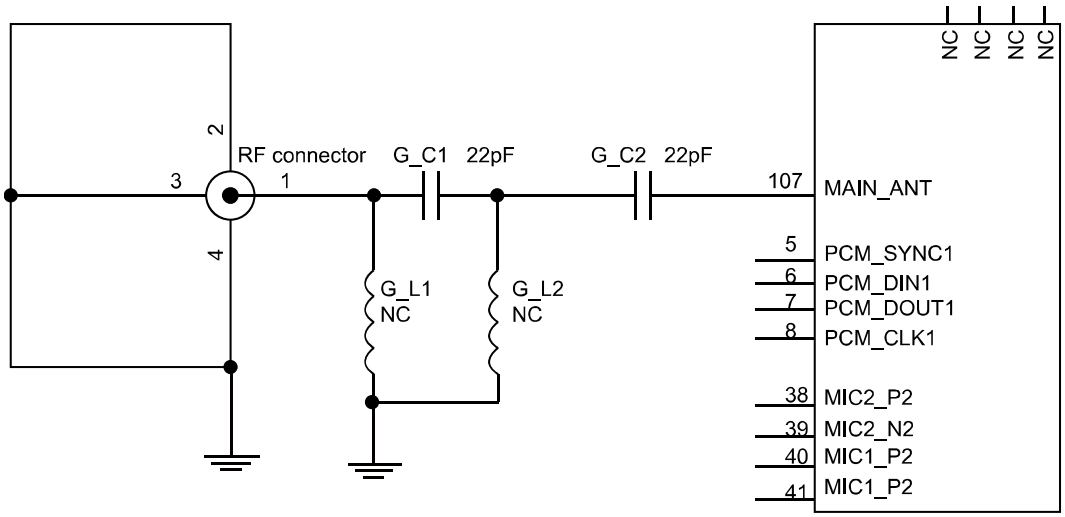
Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
107, 111, 115	Antenna interface	ANT pad size	1.5 mm × 1.0 mm	1.5 mm × 1.0 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm
107, 111, 115		ANT function	Main (pin 107)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115)

RF Signal Trace in the Main Board Design of Customers

It is recommended that you design antenna interfaces as follows:

- The antenna signal trace must be as short as possible, and controlled with 50 Ω impedance.
- The antenna interfaces pin 107, pin 111, and pin 115 should be also controlled with 50 Ω impedance.
- A π matching network must be reserved for radio frequency (RF) trace between output pins of MAIN_ANT, AUX_ANT, and GPS_ANT and antenna interfaces. There is an example of the matching network for MAIN_ANT as shown in Figure 2-13 .The components of G_C1, G_L1, and G_L2 compose a π matching network. The G_C2 is for DC blocking and matching design. The matching network for AUX_ANT and GPS_ANT are the same as the MAIN_ANT.

Figure 2-13 The matching network for MAIN_ANT



CAUTION

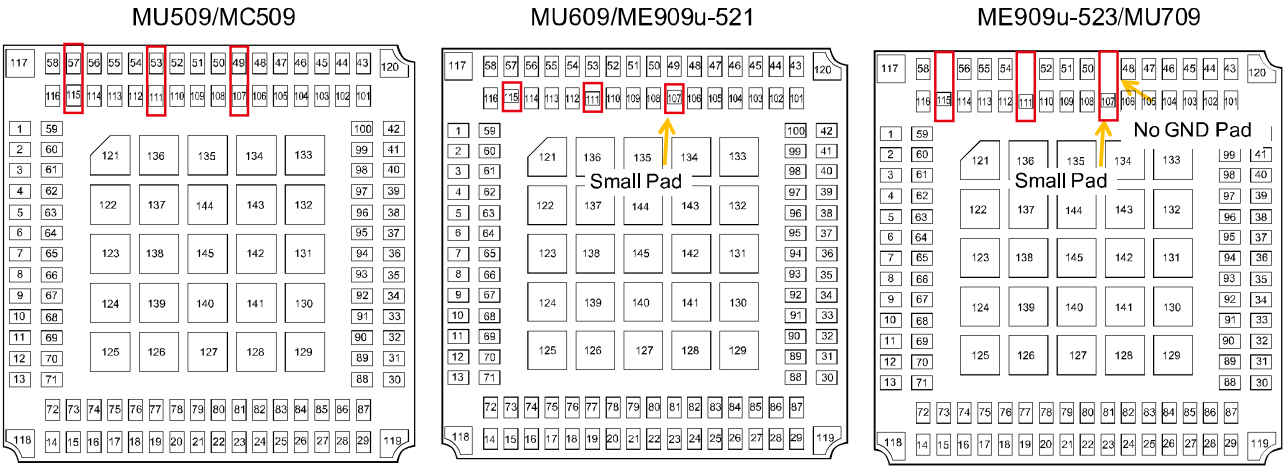
To implement 50 Ω impedance, the designer should adjust the components G_C1, G_L1, G_L2 and G_C2 shown in the preceding figure as required.

RF Interface Design for Modules

The recommended RF Pad design is shown as follows for different modules selection.

Please note that the Pad and RF trace design changes in the main board.

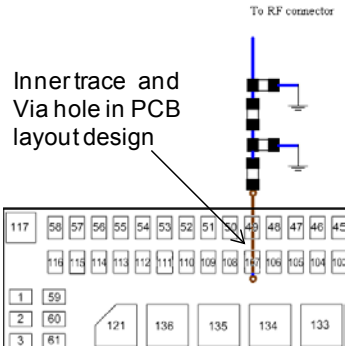
Figure 2-14 RF Pad design for different modules selection (Top view of LGA)



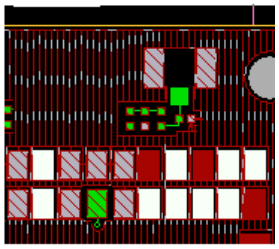
RF Trace Design

Take pin 107 for example (Top view of LGA and main board):

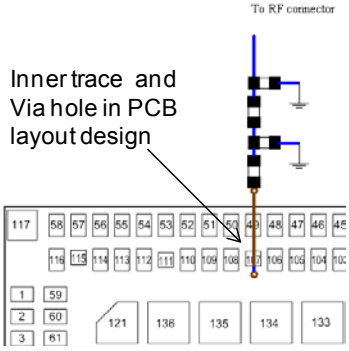
MU509/MC509



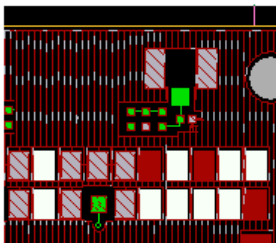
PCB layout:



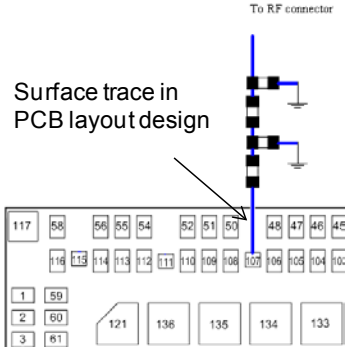
MU609/ME909u-521



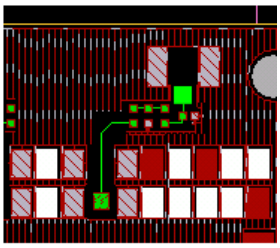
PCB layout:



ME909u-523/MU709

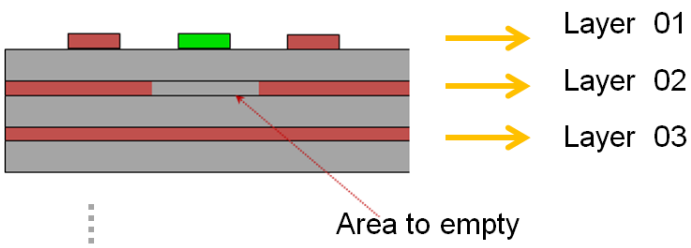


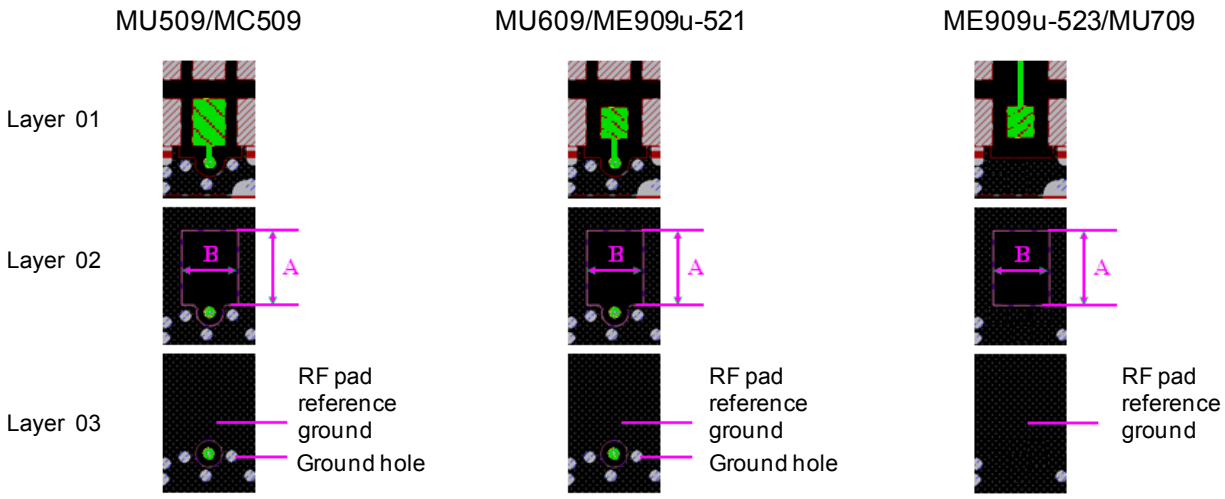
PCB layout:



RF Pad Design

Take pin 107 for example:





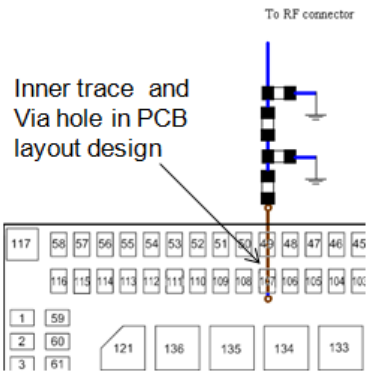
A = RF pad length + 30 mils
B = RF pad width + 30 mils

A = RF pad length + 50 mils
B = RF pad width + 40 mils

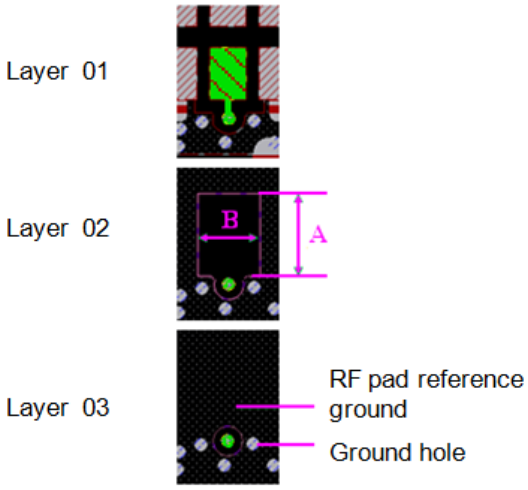
A = RF pad length + 50 mils
B = RF pad width + 40 mils

RF Interface for Module Migration Design

- MU509/MC509, MU609/ME909u-521, and ME909u-523/MU709 modules need to be compatible. We recommend that the RF interface design follow the design of MU509/MC509.

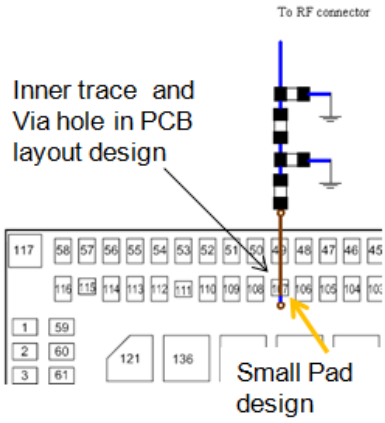


Top view of LGA and main board

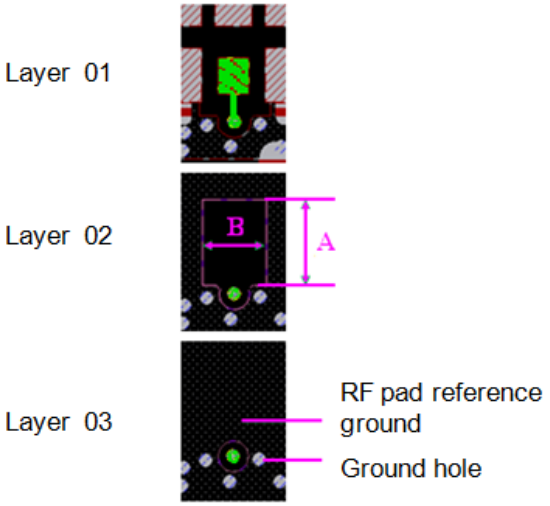


A = RF pad length + 30 mils
B = RF pad width + 30 mils

- MU609/ME909u-521 and ME909u-523/MU709 modules need to be compatible. We recommend the RF interface design follow the design of MU609/ME909u-521.



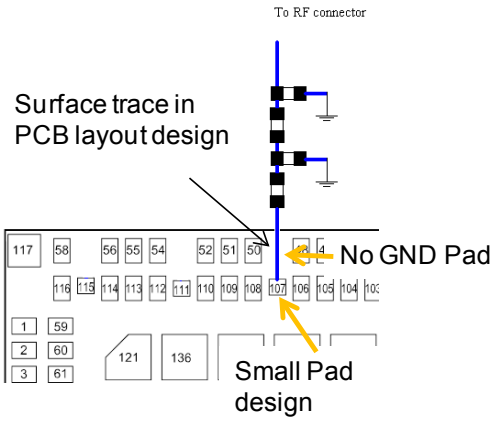
Top view of LGA and main board



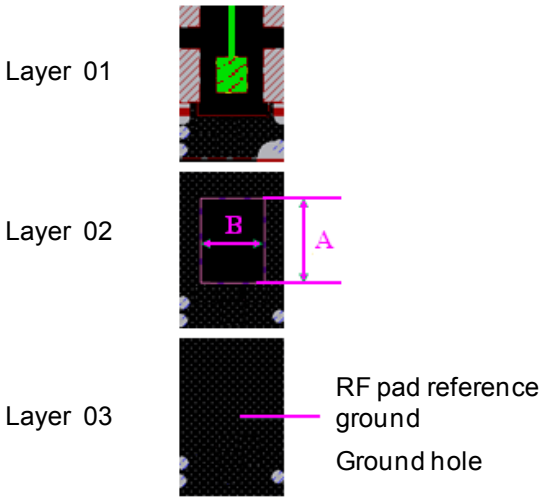
A = RF pad length + 50 mils

B = RF pad width + 40 mils

- ME909u-523/MU709 module need to be compatible. We recommend the RF interface design follow the design of ME909u-523/MU709.



Top view of LGA and main board



A = RF pad length + 50 mils

B = RF pad width + 40 mils

NOTE

- We recommend the RF interface design for different modules can accord to their own reference design.
- We recommend digging the adjacent layer below the RF pad for better RF trace impedance control.
- The pin 111 and pin 115 signal trace layout can be the same as pin 107 (MAIN_ANT).

2.6 VCC_EXT Interface Compatibility Design

2.6.1 Detailed Interface Differences

Because the signal level of MC509 and MU509 is different from MU609, MU709 and ME909u, there are two output supplies as for reference level. One is VCC_EXT2 (2.6 V), the other is VCC_EXT1 (1.8 V).

Table 2-13 Differences of the VCC_EXT interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
31	VCC_EXT	VCC_EXT2	2.6 V	2.6 V	N	N	N
32		VCC_EXT1	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V

2.7 VBAT Interface Compatibility Design

2.7.1 Detailed Interface Differences

The VBAT voltage ranges from 3.3 V to 4.2 V, with a typical value being 3.8 V. The 30 mm×30 mm LGA module provides two VBAT pads.

When the 30 mm × 30 mm LGA module works in the GSM mode, the peak current can reach 2 A. To ensure that the module works normally, place a large-capacity capacitor (1.1 mF is the best) near VBAT pads. This ensures that the VBAT voltage is not lower than 3.3 V.

All the 30 mm × 30 mm LGA modules in GSM mode (such as the MU509, MU609, MU709 and ME909u-521) must be installed with a large-capacity capacitor on the VBAT. Furthermore, five 220 μF or above energy storage capacitors are connected in parallel at the power interface of the LGA module (VBAT Pin). But for MC509, a 220 μF or above energy storage capacitors in parallel are enough.

Table 2-14 Differences of capacitors in parallel at the VBAT Pin

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
12, 13	Power interface	VBAT (3.3 V–4.2 V)	Five 220 μF capacitors needed	A 220 μF capacitors needed	Five 220 μF capacitors needed	Five 220 μF capacitors needed	Five 220 μF capacitors needed

2.7.2 VBAT Interface Design Guide

It is recommended that you add ferrite beads and five 220 μF capacitors (A 220 μF capacitors for MC509) are connected in parallel at VBAT Pin to the power circuit. The diagram of recommended circuit is shown in the following figures.

Figure 2-15 Recommended power circuit of MU509/MU609/ME909u/MU709 module

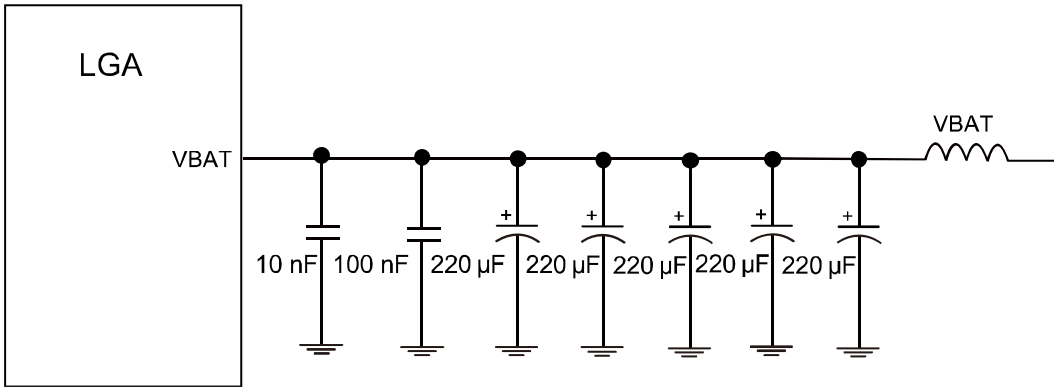
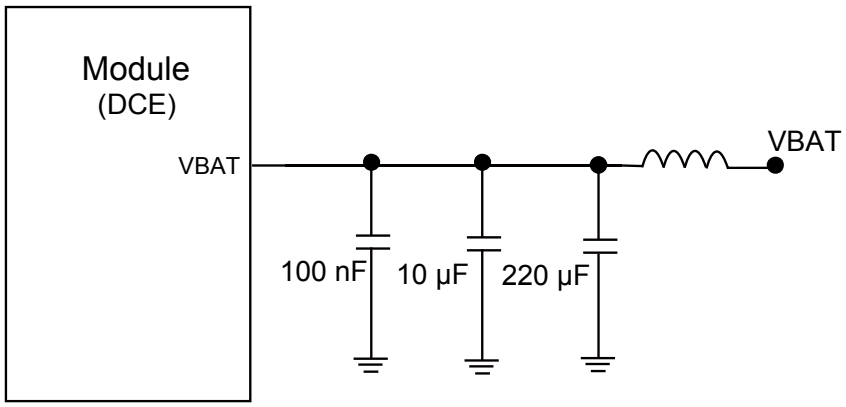


Figure 2-16 Recommended power circuit of MC509 module



2.8 JTAG Interface Compatibility Design

2.8.1 Detailed Interface Differences

Please note that JTAG level (CMOS 2.6 V) of MC509 is different from JTAG level (CMOS 1.8 V) of MU509/MU609/ME909u/MU709.

Table 2-15 Differences of the JTAG signal

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
30	JTAG	JTAG_TMS	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
36		JTAG_TRST_N	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
42		JTAG_TCK	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
72		JTAG_TDO	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
87		JTAG_TDI	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
93		JTAG_RTCK	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	Reserved
14		PS_HOLD	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	Reserved
100/ 47		RESIN_N/JTAG_SRST_N	CMOS 1.8 V (pin 100)	CMOS 1.8 V (pin 100)	CMOS 1.8 V (pin 100)	**JTAG_SRST_N (pin 47) reset for JTAG debugging**	N

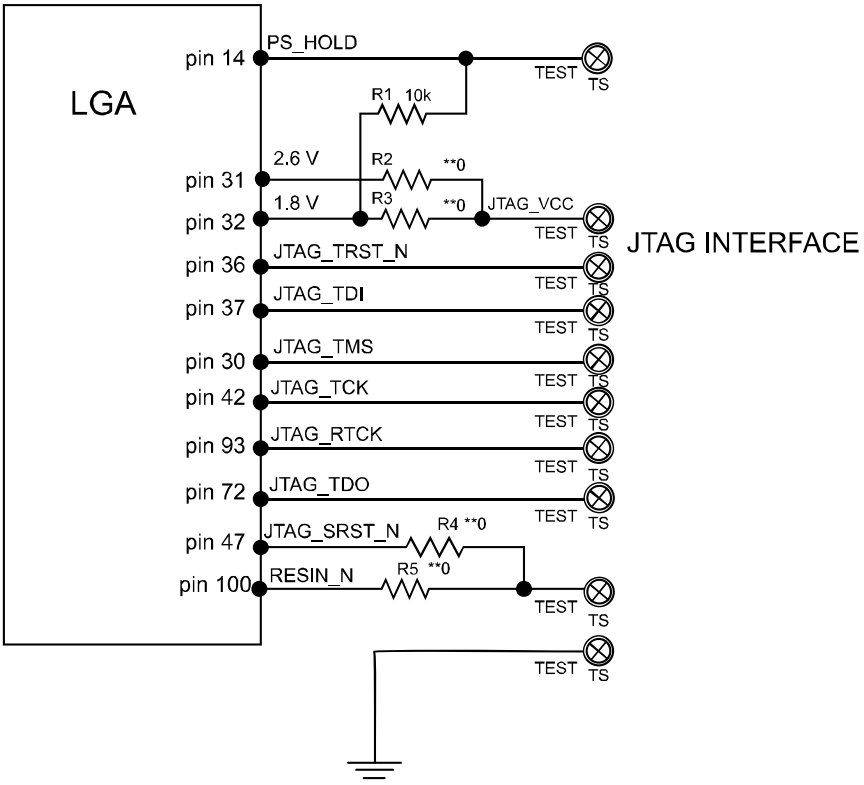
2.8.2 JTAG Interface Design Guide

To facilitate fault location, it is recommended that you lead out JTAG signals from test points. The LGA module must be reserved with JTAG test point interfaces for fault analysis and location. The JTAG interface signals include the following signals. Arrange test points according to the following relationship.

The following figure shows the connections of JTAG signal pins.

Figure 2-17 Circuit of the JTAG interface

When you want 30 mm×30 mm LGA module in JTAG mode, please Install R1;
When you want 30 mm×30 mm LGA module in normal mode, please do not install R1;
For MC509, install R2 and do not install R3;
For MU509/MU609/ME909u/MU709, install R3 and do not install R2



For ME909u, install R4 and do not install R5;
For MC509/MU509/MU609/MU709,
install R5 and do not install R4

2.9 UART Interface Compatibility Design

2.9.1 Detailed Interface Differences

Please note that the different signal level of UART between MU509/MC509 and MU609/ME909u/MU709. The signal level of MU509 and MC509 is CMOS 2.6 V and MU609, MU709 and ME909u is CMOS 1.8 V. Therefore, you must consider compatibility during circuit designing.

ME909u do not support 8-wire line UART. It only supports 2 × 4-wire line UARTs and a 2-wire UART (only for debugging).

Table 2-16 Differences of the UART interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
73	UART	UART0_DSR	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	Reserved	CMOS 1.8 V
74		UART0_RTS	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
75		UART0_DCD	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	Reserved	CMOS 1.8 V
76		UART0_TX	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
77		UART0_RING	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	Reserved	CMOS 1.8 V
78		UART0_RX	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
79		UART0_DTR	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	Reserved	CMOS 1.8 V
80		UART0_CTS	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
1		UART1_TX	N	N	CMOS 1.8 V for debugging	CMOS 1.8 V	CMOS 1.8 V for debugging
2		UART1_RTS	N	N	N		N
3		UART1_CTS	N	N	N		N
4		UART1_RX	N	N	CMOS 1.8 V for debugging		CMOS 1.8 V for debugging
28		UART2_TX	Reserved	Reserved	Reserved	CMOS 1.8 V For debugging	Reserved
29		UART2_RX	Reserved	Reserved	Reserved	CMOS 1.8 V For debugging	Reserved

Note:
- N=not supported
- Y=supported

2.9.2 UART Interface Design Guide

CAUTION

Besides compatibility of the UART, designer must consider the time sequence of signals. The UART signals externally connected with the LGA module must be transmitted at least 3s after the LGA module is powered on. Otherwise, a sink current occurs and the LGA module may be improperly powered on.

Figure 2-18 The recommended connection of the UART0 interface in the module (DCE) with the host (DTE)

For MU509 and MC509, install R1,R3,R4,R5,R6, and do not install R2;
For MU609 and MU709, install R2,R3,R4,R5,R6, and do not install R1.
For ME909u, install R2, and do not install R1,R3,R4,R5,R6.
VCC_EXT level is the same with DTE UART signal.

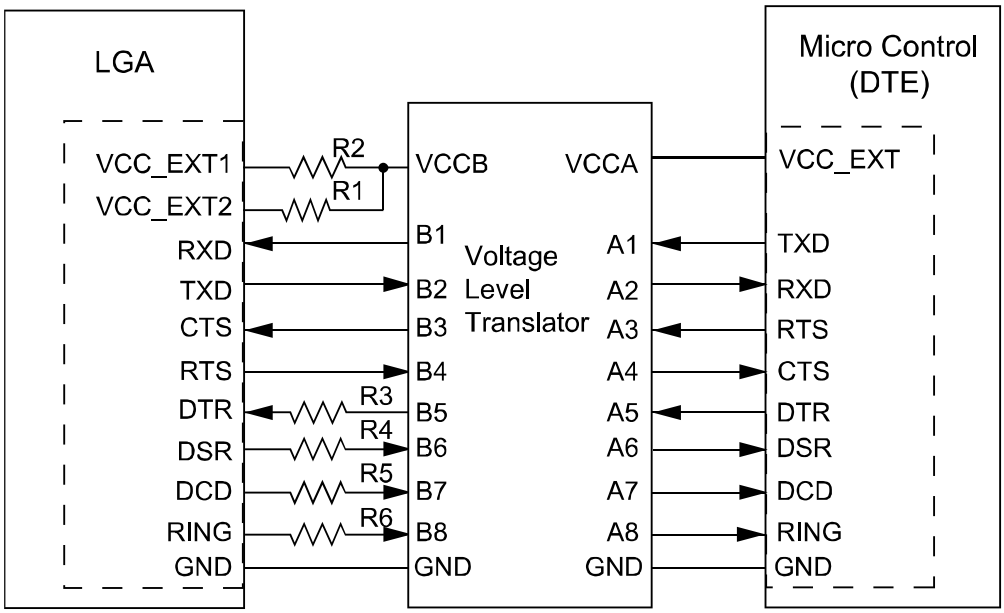


Figure 2-19 The recommended connection of the UART1 interface in the module (DCE) with the host (DTE)

For MU509 and MC509, do not install R1,R2,R3,R4,R5,R6;
For MU609 and MU709 for debugging, install R2,R3,R4, and do not install R1,R5,R6.
For ME909u, install R2, R3,R4,R5,R6, and do not install R1.
VCC_EXT level is the same with DTE UART signal.

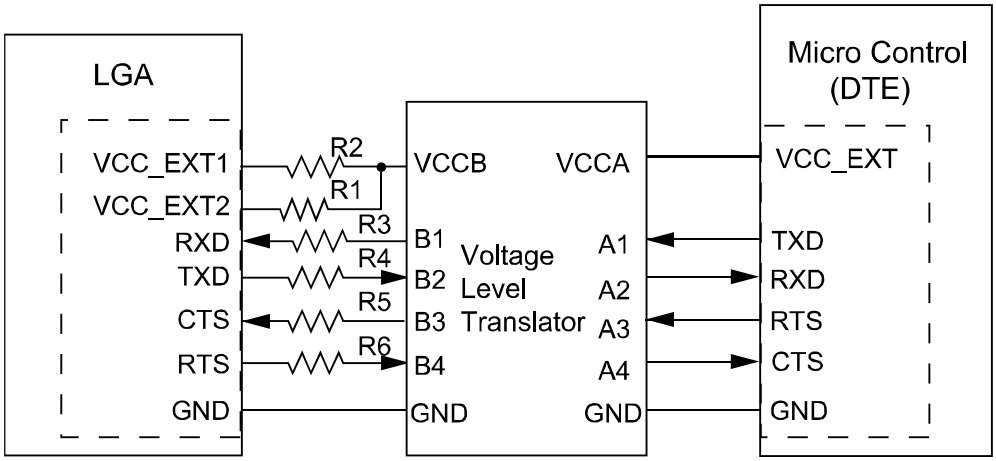
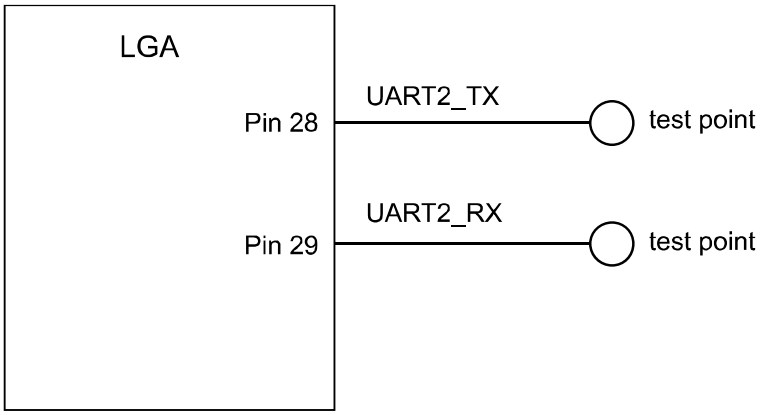


Figure 2-20 Circuit diagram of the UART2 interface (only for debugging)



2.10 USB Interface Compatibility Design

2.10.1 Detailed Interface Differences

Please note that only MU609, MU709 and ME909u support USB 2.0 High Speed. MC509 and MU509 do not support USB 2.0 High Speed.

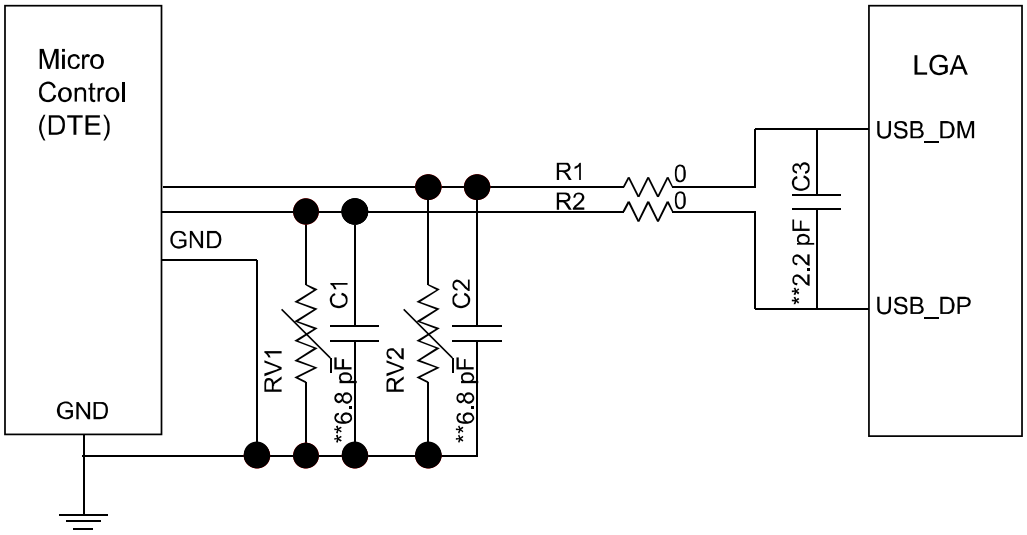
Table 2-17 Differences of the USB interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
85	USB	USB_DM	USB 2.0 Full Speed	USB 2.0 Full Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed
86		USB_DP	USB 2.0 Full Speed	USB 2.0 Full Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed

2.10.2 USB Interface Design Guide

The following figure shows recommended circuit of USB interface.

Figure 2-21 Recommended circuit of USB interface



Requirements for USB signal layout and traces:

1. USB_DM and USB_DP are required to control the differential impedance 90 Ω.
2. R1 and R2 are ready for dealing with impedance matching. You can adjust the value of R1 or R2 in order that the differential impedance of the USB signal should be 90 ohm.
3. The length of the gap between USB_DM and USB_DP should not exceed 5mil.
4. The USB differential signal trace must be as short as possible, and laid out away from high-speed clock signals and other periodic signals as far as possible.
5. Minimize through-holes and turning angles on the USB signal trace to reduce signal reflection and impedance change.
6. Do not route the USB signal trace under the following components: crystal, oscillator, clock circuit, electromagnetic component, and I C that uses or generates clocks.
7. Avoid stubs on the USB signal trace because stubs generate reflection and affect the signal quality.

8. Route the USB signal trace on a complete reference plane (GND) and avoid crossing inter-board gaps because inter-board gaps cause a large reflow channel area and increase inductance and radiation. In addition, avoid signal traces on different layers.
9. The USB signal trace must be far away from core logical components because the high current pulse is generated during the state transitions process of core components may impose interference on signals.
10. The USB signal trace must be far away from board edges with a minimum distance of 20 × h (h indicates the vertical distance between the trace and the reference layer) to avoid signal radiation.
11. C1 and C2 are ready for dealing with filter differential mode interference and C3 is ready for dealing with filter common mode interference. You can choose the value of the C1, C2 and C3 according to the actual PCB which is integrated 30 mm×30 mm LGA Module.

NOTE
"**" means do not install at first, but C1, C2 and C3 need to reserve the capacitor pads in order to deal with filter common and differential mode interference.

2.11 LED Interface Compatibility Design

2.11.1 Detailed Interface Differences

Table 2-18 Differences of LED control signal

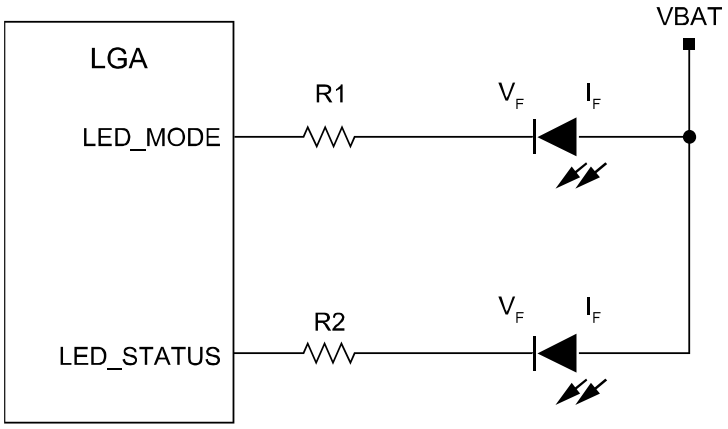
Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
91	LED	LED_STATUS	Y	Y	Reserved (Planning for LED)	Reserved (Planning for LED)	Reserved (Planning for LED)
101		LED_MODE	Y	Y	Y	Y	Y

2.11.2 LED Interface Design Guide

Pin 91 and pin 101 are worked as LED control signals, which are the current sink type; the drive strength is 10 mA.

For the pins of current sink type, it is recommended that you connect the pins based on the circuit diagram shown in the following figure. R1 and R2 can be adjusted according to the actual LED brightness. The VCC voltage must not exceed VBAT +0.5 V; otherwise, the internal chip of a module may be damaged. It is recommended that you use the VBAT as the VCC.

Figure 2-22 Circuit of the LED interface



2.12 ADC Interface Compatibility Design

2.12.1 Detailed Interface Differences

Table 2-19 Differences of ADC signal

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
102	ADC	ADC_1	N	N	N	Y[1]	N
104		ADC_2	N	N	N	Y[1]	N

NOTE
[1]: The ME909u-523 module provides two ADC interfaces. ME909u-521 does not support ADC interface at present (The firmware is being developed).

3 Mechanical Specifications Compatibility Design Guide

3.1 About This Chapter

- Dimensions Differences
- Customer PCB Design
- Assembly Processes

3.2 Dimensions Differences

Table 3-1 shows the dimension differences of Huawei 30 mm × 30 mm LGA modules.

It is recommended that the reserved height is 2.65 mm ± 0.20 mm (height of MC509, which is the highest of four LGA modules) for compatibility design.

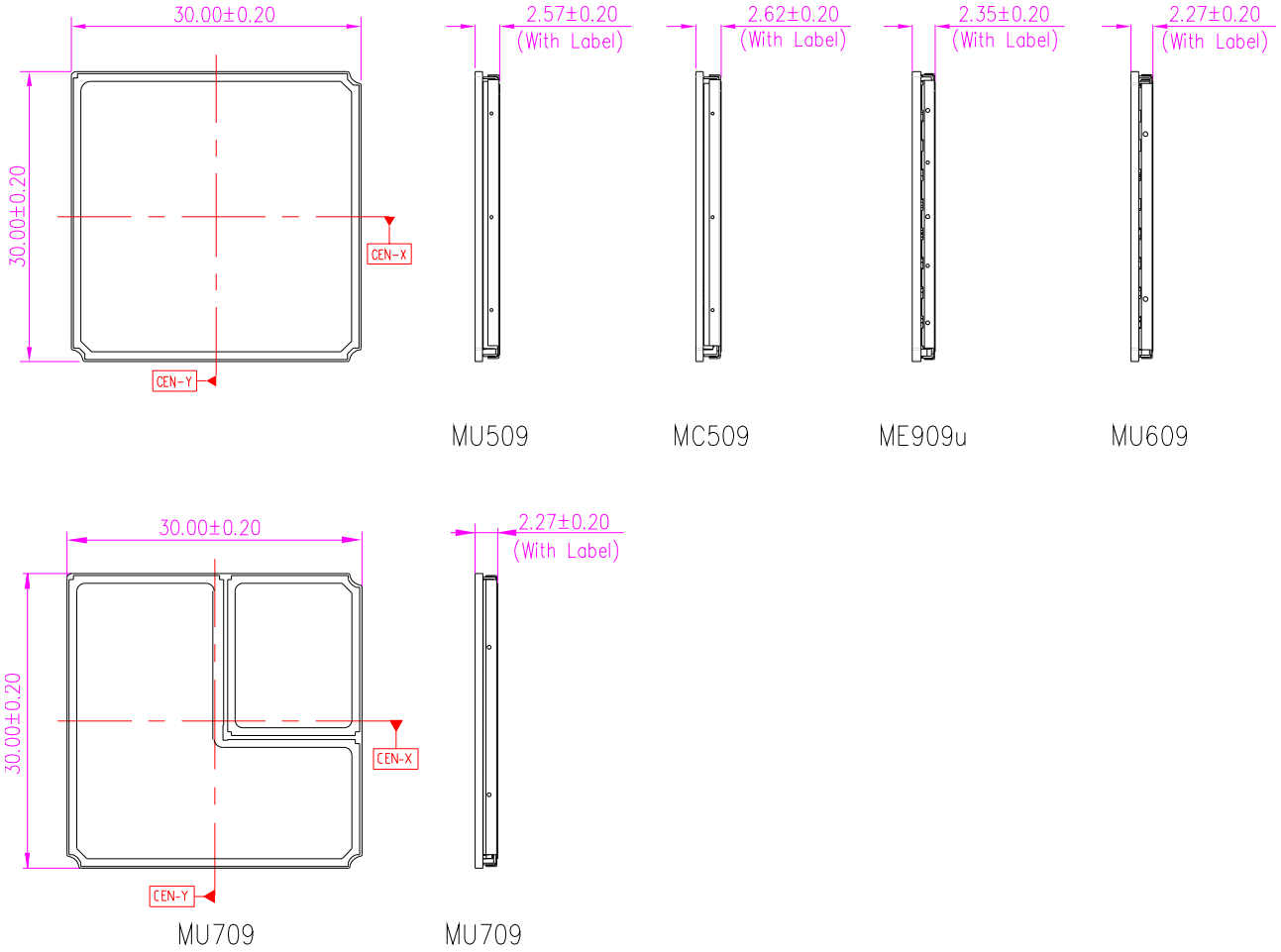
For full compatibility, please design the layout referring to MC509 size (30 mm × 30 mm × 2.65 mm ± 0.20 mm).

Table 3-1 Differences of LGA module size

LGA module	Dimension	Unit
MU509	30 × 30 × 2.57	mm
MC509	30 × 30 × 2.65	mm
MU609	30 × 30 × 2.27	mm
ME909u	30 × 30 × 2.35	mm
MU709	30 × 30 × 2.27	mm

Figure 3-1 shows the dimensions of Huawei 30 mm × 30 mm LGA modules.

Figure 3-1 Dimensions of Huawei 30 mm × 30 mm LGA modules (Unit: mm)

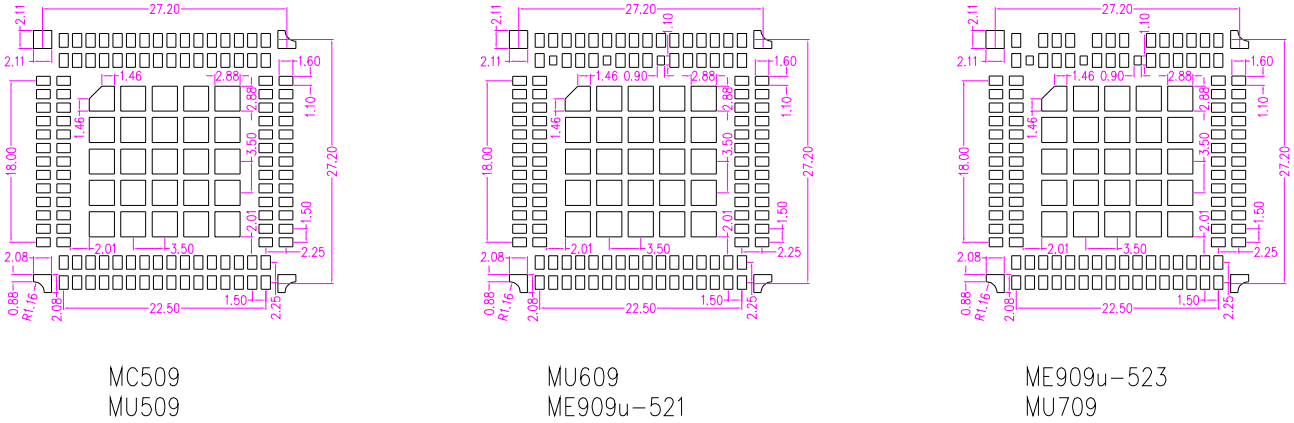


3.3 Customer PCB Design

3.3.1 PCB Pad Design

To achieve assembly yields and solder joints of high reliability, it is recommended that the PCB pad size be designed as follows:

Figure 3-2 The footprint design of Huawei 30 mm × 30 mm LGA modules (Unit: mm)



Please note that the differences of PCB pad among 30 mm × 30 mm LGA modules.

- The 49 pin, 53 pin and 57 pin of MU709 and ME909u-523 are empty.
- The pad size and function of the antenna interface among 30 mm × 30 mm LGA modules are different, as shown in Table 3-2 .

Table 3-2 Differences of the antenna interface in pad size and function

Pin No.	Interface	Name	MU509	MC509	MU609	ME909u	MU709
107, 111, 115	Antenna interface	ANT pad size	1.5 mm × 1.0 mm	1.5 mm × 1.0 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm
107, 111, 115		ANT function	Main (pin 107)	Main (pin107), AUX (pin115), GPS (pin 111)	Main (pin107), AUX (pin115), GPS (pin 111)	Main (pin107), AUX (pin115), GPS (pin 111)	Main (pin107), AUX (pin115)

3.3.2 Requirements on PCB Layout

- To reduce deformation, a thickness of at least 1.0 mm is recommended.
- Other devices must be located more than 3 mm (5 mm recommended) away from the LGA module. The minimum distance between the LGA module and the PCB edge is 0.5 mm.
- When the PCB layout is double sided, the module must be placed on the second side for assembly; so as to avoid module dropped from PCB or component (located in module) re-melding defects caused by uneven weight.

3.4 Assembly Processes

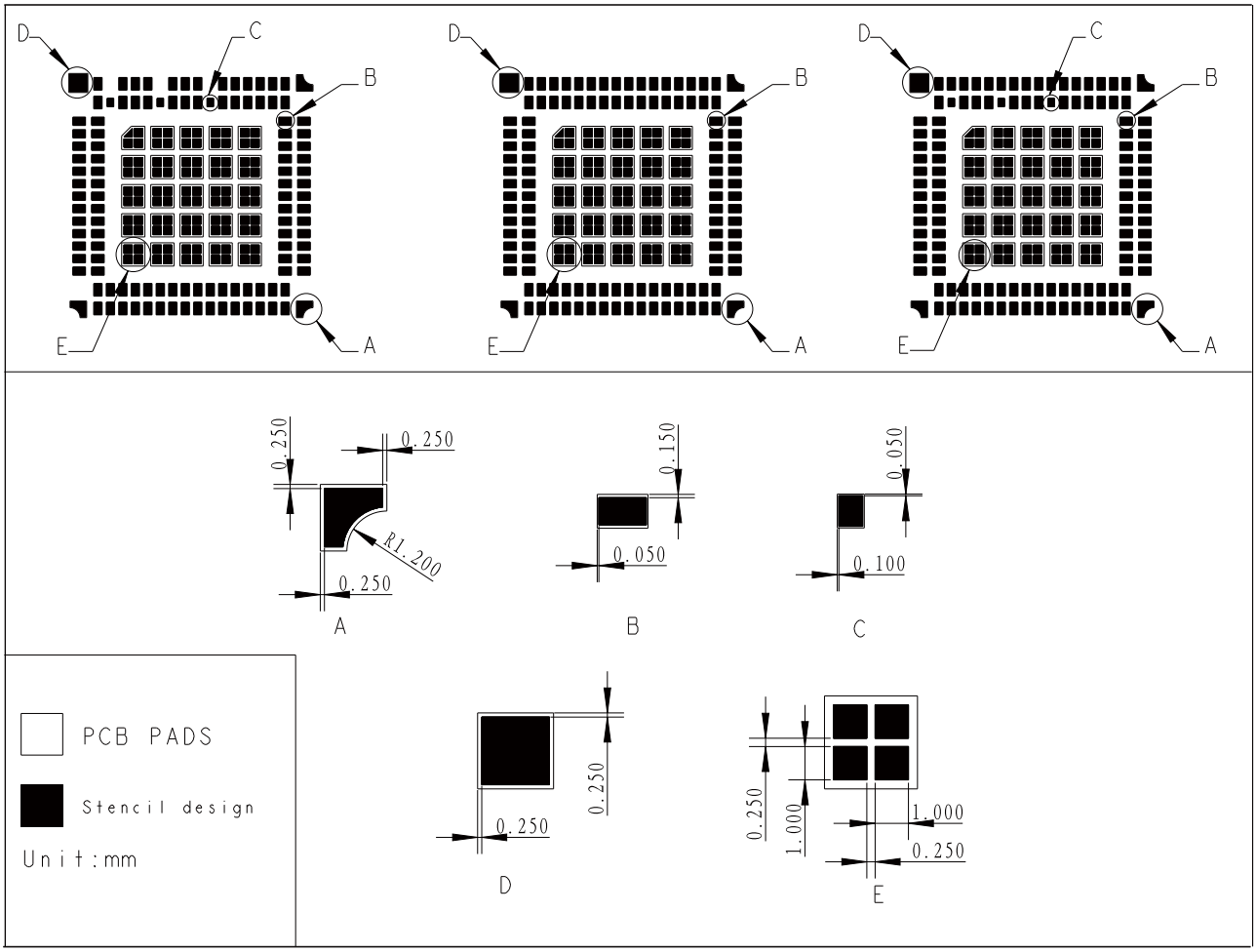
3.4.1 General Description of Assembly Processes

- Tray modules are required at SMT lines, because 30 mm × 30 mm LGA modules are placed on ESD pallets.
- Reflow ovens with at least seven temperature zones are recommended, the reflow profile please refer to Figure 3-4 .

3.4.2 Stencil Design

It is recommended that the stencil for the 30 mm × 30 mm LGA modules be 0.15 mm in thickness. For the stencil design, see Figure 3-3 .

Figure 3-3 Recommended stencil design of LGA module



3.4.3 Reflow Profile

For the soldering temperature of the 30 mm × 30 mm LGA modules, see the following figure.

Figure 3-4 Reflow profile

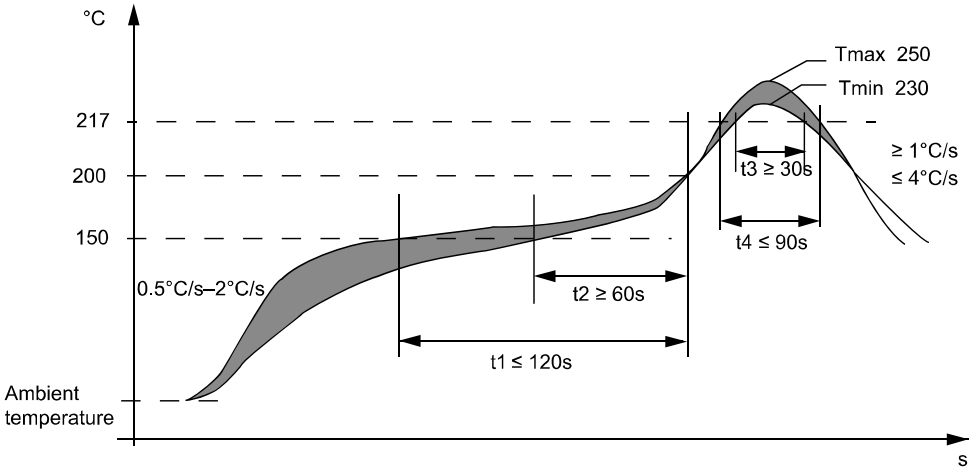


Table 3-3 Reflow parameters

Temperature Zone	Time	Key Parameter
Preheat zone (40°C–150°C)	60s–120s	Heating rate: 0.5°C/s–2°C/s
Soak zone (150°C–200°C)	(t1–t2): 60s–120s	Heating rate: < 1.0°C/s
Reflow zone (> 217°C)	(t3–t4): 30s–90s	Peak reflow temperature: 230°C–250°C
Cooling zone	Cooling rate: 1°C/s ≤ Slope ≤ 4°C/s	

4 Appendix

Table 4-1 Definition of LGA Interfaces

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
1	NC	-	NC	-	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V
2	NC	-	NC	-	NC	-	UART1_RTS	CMOS 1.8 V	UART1_RTS	CMOS 1.8 V	NC	-
3	NC	-	NC	-	NC	-	UART1_CTS	CMOS 1.8 V	UART1_CTS	CMOS 1.8 V	NC	-
4	NC	-	NC	-	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V
5	PCM_SYNC	CMOS 2.6 V	PCM_SYNC	CMOS 2.6 V	PCM_SYNC	CMOS 1.8 V	PCM_SYNC	CMOS 1.8 V	PCM_SYNC	CMOS 1.8 V	PCM_SYNC	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
6	PCM_DIN	CMOS 2.6 V	PCM_DIN	CMOS 2.6 V	PCM_DIN	CMOS 1.8 V	PCM_DIN	CMOS 1.8 V	PCM_DIN	CMOS 1.8 V	PCM_DIN	CMOS 1.8 V
7	PCM_DOUT	CMOS 2.6 V	PCM_DOUT	CMOS 2.6 V	PCM_DOUT	CMOS 1.8 V	PCM_DOUT	CMOS 1.8 V	PCM_DOUT	CMOS 1.8 V	PCM_DOUT	CMOS 1.8 V
8	PCM_CLK	CMOS 2.6 V	PCM_CLK	CMOS 2.6 V	PCM_CLK	CMOS 1.8 V	PCM_CLK	CMOS 1.8 V	PCM_CLK	CMOS 1.8 V	PCM_CLK	CMOS 1.8 V
9	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA1	CMOS 3.0 V
10	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA2	CMOS 3.0 V
11	WAKEUP_IN	CMOS 2.6 V	WAKEUP_IN	CMOS 2.6 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V
12	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V
13	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V
14	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V
15	Reserved (Planning for SLEEP_STATUS) CMOS2.6 V	-	Reserved (Planning for SLEEP_STATUS) CMOS2.6 V	-	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V
16	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
17	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-
18	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-
19	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-
20	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-
21	NC		NC		NC	-	ANT_TUNE 0	CMOS 1.8 V	ANT_TUNE 0	CMOS 1.8 V	NC	-
22	NC		NC		NC	-	ANT_TUNE 1	CMOS 1.8 V	ANT_TUNE 1	CMOS 1.8 V	NC	-
23	NC		NC		NC	-	ANT_TUNE 2	CMOS 1.8 V	ANT_TUNE 2	CMOS 1.8 V	NC	-
24	NC		NC		NC	-	ANT_TUNE 3	CMOS 1.8 V	ANT_TUNE 3	CMOS 1.8 V	NC	-
25	NC		NC		NC	-	NC	-	NC	-	NC	-
26	NC		NC		NC	-	NC	-	NC	-	NC	-
27	NC		NC		NC	-	Reserved	-	Reserved	-	NC	-
28	Reserved	-	Reserved	-	Reserved	-	UART2_TX	CMOS 1.8 V	UART2_TX	CMOS 1.8 V	Reserved	-
29	Reserved	-	Reserved	-	Reserved	-	UART2_RX	CMOS 1.8 V	UART2_RX	CMOS 1.8 V	Reserved	-
30	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 2.6 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
31	VCC_EXT2	2.6 V	VCC_EXT2	2.6 V	NC	-	NC	-	NC	-	Reserved	-
32	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V
33	NC		NC		NC	-	NC	-	NC	-	NC	-
34	SIM _VCC	1.8 V/2.85 V	RUIM_VCC	1.8 V/2.85 V	SIM_VCC	1.8 V/2.85 V	SIM_VCC	1.8 V/2.85 V	SIM_VCC	1.8 V/2.85 V	USIM_VCC	1.8 V/3.0 V
35	VCOIN		VCOIN		Reserved	-	Reserved	-	Reserved	-	Reserved	-
36	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 2.6 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V
37	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
38	MIC2_P		MIC2_P		NC	-	NC	-	NC	-	NC	-
39	MIC2_N		MIC2_N		NC	-	NC	-	NC	-	NC	-
40	MIC1_P		MIC1_P		NC	-	NC	-	NC	-	NC	-
41	MIC1_N		MIC1_N		NC	-	NC	-	NC	-	NC	-
42	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 2.6 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V
43	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
44	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	Reserved	-	Reserved	-	Reserved	-	Reserved	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
45	GPIO	CMOS 2.6 V	W_DISABLE	CMOS 2.6 V	Reserved (Planning for W_DISABLE) CMOS 1.8 V	-	Reserved (Planning for W_DISABLE) CMOS 1.8 V	-	Reserved (Planning for W_DISABLE) CMOS 1.8 V	-	Reserved (Planning for W_DISABLE) CMOS 1.8 V	-
46	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	Reserved	-	Reserved	-	Reserved	-	Reserved	-
47	NC	-	NC	-	NC	-	JTAG_SRST_N	CMOS 1.8 V	JTAG_SRST_N	CMOS 1.8 V	NC	-
48	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
49	GND	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-
50	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
51	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V
52	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
53	GND	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-
54	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
55	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V
56	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
57	GND	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-
58	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
59	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
60	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
61	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
62	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
63	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
64	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
65	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
66	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA3	CMOS 3.0 V
67	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_CLK	CMOS 3.0 V
68	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA0	CMOS 3.0 V
69	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_CMD	CMOS 3.0 V
70	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
71	WAKEUP_OUT	CMOS 2.6 V	WAKEUP_OUT	CMOS 2.6 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
72	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 2.6 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V
73	UART0_DSR	CMOS 2.6 V	UART0_DSR	CMOS 2.6 V	UART0_DSR	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DSR	CMOS 1.8 V
74	UART0_RTS	CMOS 2.6 V	UART0_RTS	CMOS 2.6 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V
75	UART0_DCD	CMOS 2.6 V	UART0_DCD	CMOS 2.6 V	UART0_DCD	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DCD	CMOS 1.8 V
76	UART0_TX	CMOS 2.6 V	UART0_TX	CMOS 2.6 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V
77	UART0_RING	CMOS 2.6 V	UART0_RING	CMOS 2.6 V	UART0_RING	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_RING	CMOS 1.8 V
78	UART0_RX	CMOS 2.6 V	UART0_RX	CMOS 2.6 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V
79	UART0_DTR	CMOS 2.6 V	UART0_DTR	CMOS 2.6 V	UART0_DTR	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DTR	CMOS 1.8 V
80	UART0_CTS	CMOS 2.6 V	UART0_CTS	CMOS 2.6 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V
81	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module
82	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
83	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
84	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
85	USB_DM		USB_DM		USB_DM	-	USB_DM	-	USB_DM	-	USB_DM	-
86	USB_DP		USB_DP		USB_DP	-	USB_DP	-	USB_DP	-	USB_DP	-
87	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 2.6 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V
88	SIM_RESET	1.8 V/2.85 V	RUIM_RESET	1.8 V/2.85 V	SIM_RESET	1.8 V/2.85 V	SIM_RESET	1.8 V/2.85 V	SIM_RESET	1.8 V/2.85 V	USIM_RESET	1.8 V/3.0 V
89	SIM_DATA	1.8 V/2.85 V	RUIM_DATA	1.8 V /2.85 V	SIM_DATA	1.8 V /2.85 V	SIM_DATA	1.8 V /2.85 V	SIM_DATA	1.8 V/2.85 V	USIM_DATA	1.8 V/3.0 V
90	SIM_CLK	1.8 V/2.85 V	RUIM_CLK	1.8 V/2.85 V	SIM_CLK	1.8 V/2.85 V	SIM_CLK	1.8 V/2.85 V	SIM_CLK	1.8 V/2.85 V	USIM_CLK	1.8 V/3.0 V
91	LED_STATUS	SINK	LED_STATUS	SINK	Reserved (Planning for LED)	-	Reserved (Planning for LED)	-	Reserved (Planning for LED)	-	Reserved (Planning for LED)	-
92	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_VCC	3.0 V
93	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 2.6 V	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 1.8 V	NC	-
94	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
95	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
96	EAR_OUT_N	-	EAR_OUT_N		NC	-	NC	-	NC	-	NC	-
97	EAR_OUT_P	-	EAR_OUT_P		NC	-	NC	-	NC	-	NC	-
98	SPKR_OUT_P	-	SPKR_OUT_P		NC	-	NC	-	NC	-	NC	-
99	SPKR_OUT_N	-	SPKR_OUT_N		NC	-	NC	-	NC	-	NC	-
100	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	NC	-
101	LED_MODE	SINK	LED_MODE	SINK	LED_MODE	SINK	LED_MODE (The firmware with this feature is being developed.)	SINK	LED_MODE (The firmware with this feature is being developed.)	SINK	LED_MODE	SINK
102	NC	-	NC	-	Reserved	-	Reserved	-	ADC_1	-	Reserved	-
103	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
104	NC	-	NC	-	NC	-	Reserved		ADC_2	-	Reserved	-
105	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V
106	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
107	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-
108	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
109	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V
110	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
111	NC	-	GPS_ANT	-	GPS_ANT	-	GPS_ANT	-	GPS_ANT	-	NC	-
112	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
113	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V
114	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
115	NC	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-
116	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
117	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
118	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
119	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
120	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
121	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
122	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
123	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
124	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
125	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
126	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
127	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
128	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
129	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
130	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
131	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
132	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
133	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
134	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
135	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
136	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
137	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
138	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
139	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
140	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
141	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523		MU709	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
142	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
143	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
144	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
145	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Note:

- The NC pins are not connected, therefore, before you deal with these pins, please refer to the corresponding hardware guide.
- The Reserved pins are internally connected to the modules. Therefore, these pins should not be used, otherwise they may cause problems. Please contact with us for more details about this information.

Figure 4-2 Top view of sequence of MU509 and MC509 interface pins

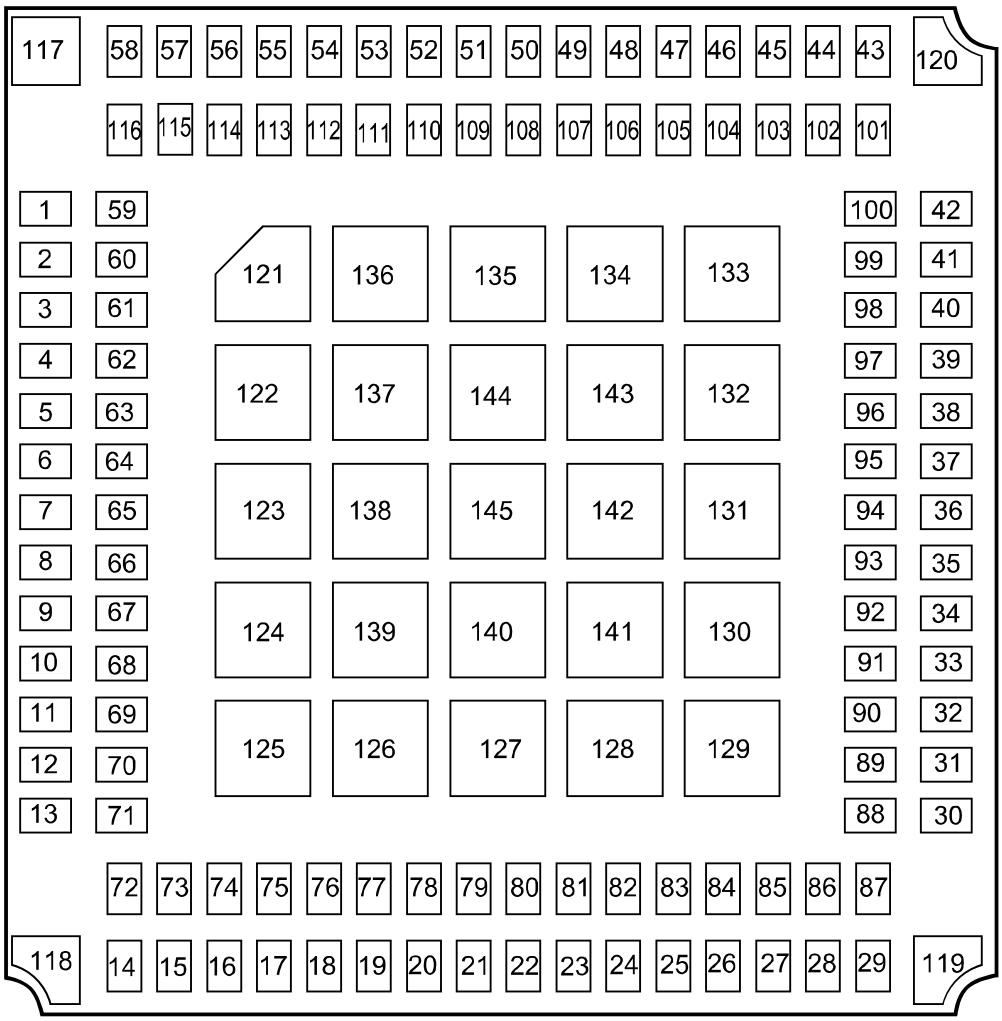


Figure 4-3 Top view of sequence of MU609 and ME909u-521 interface pins

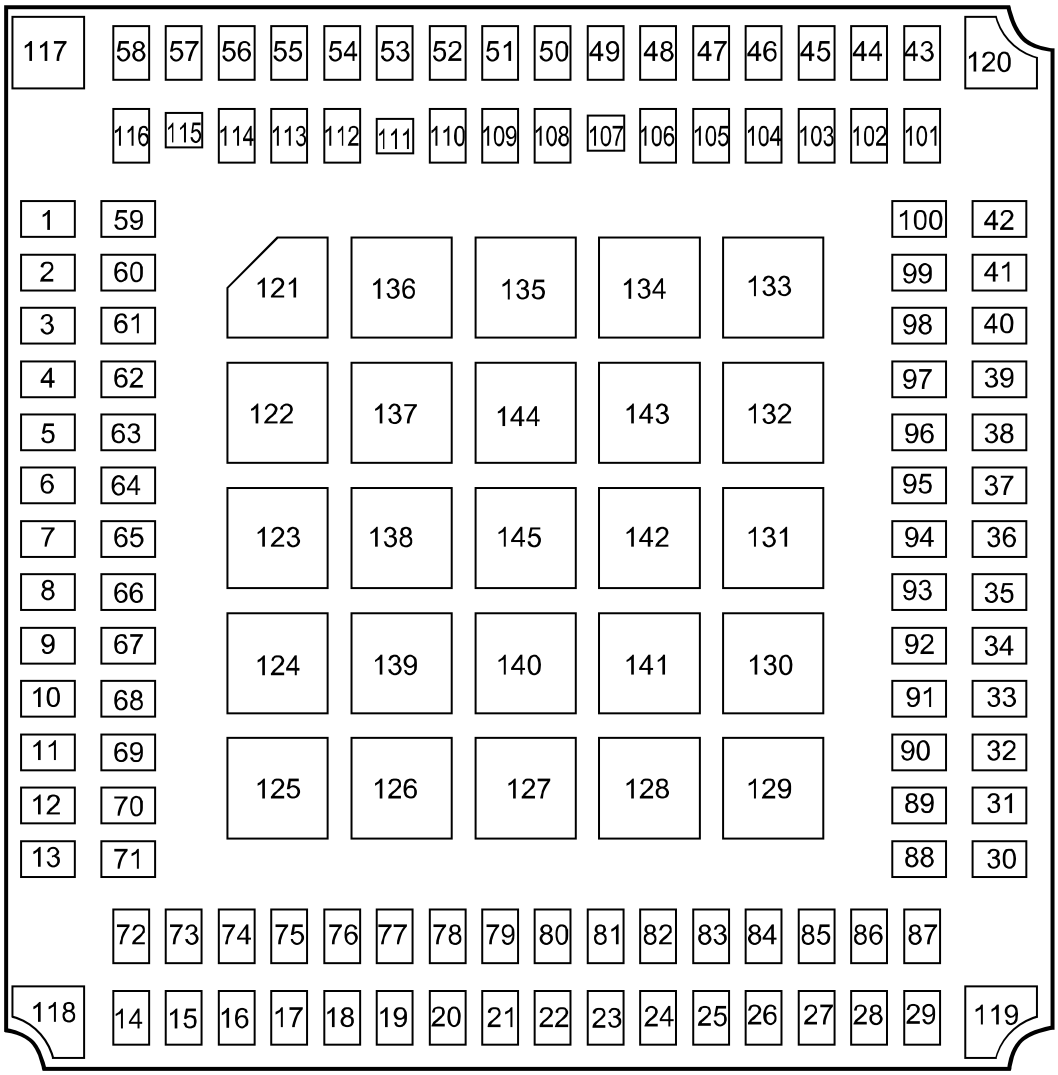
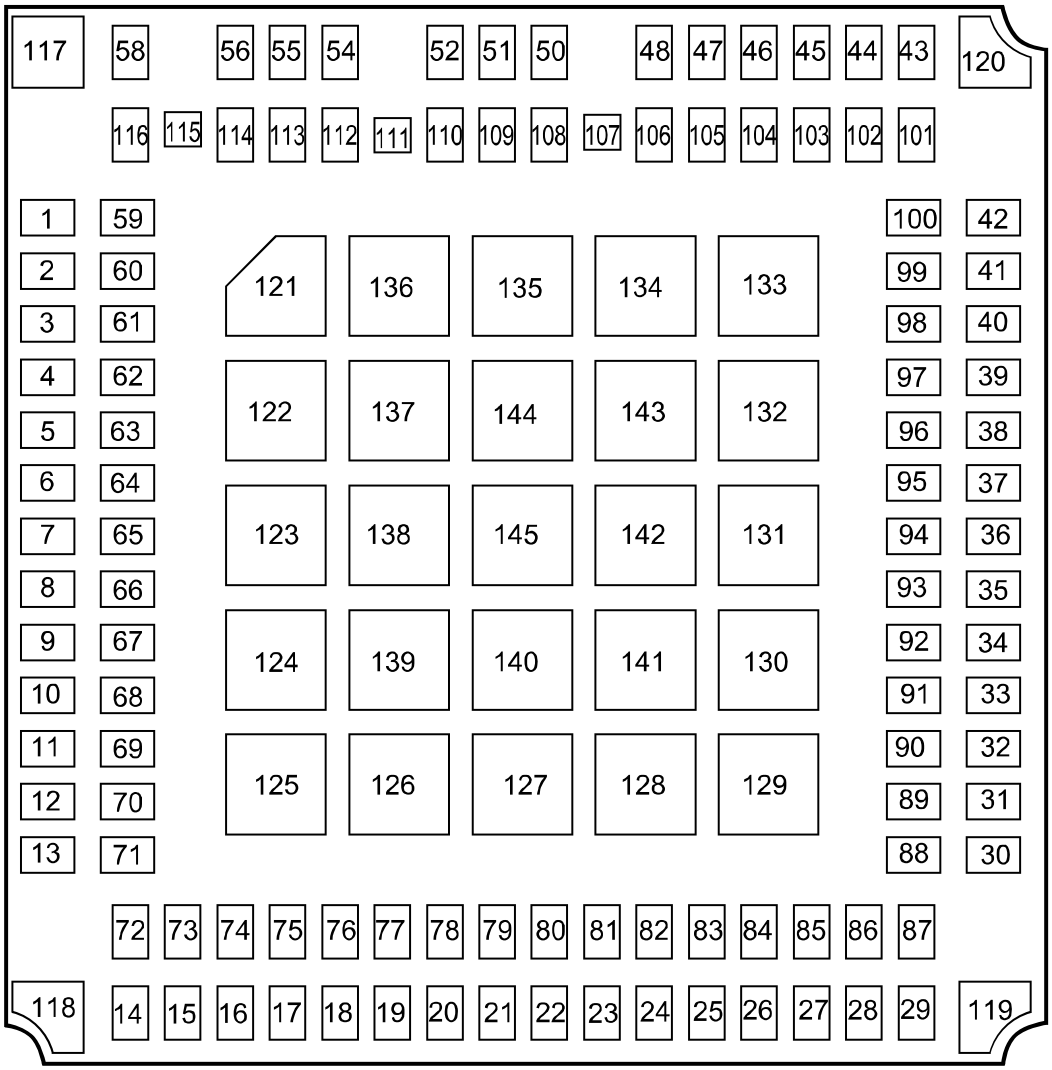


Figure 4-4 Top view of sequence of MU709 and ME909u-523 interface pins



5 Acronyms and Abbreviations

Acronym or Abbreviation	Expansion
AUX	Auxiliary
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
DC	Direct Current
DCE	Data Communication Equipment
DL	Down Link
DTE	Data Terminal Equipment
EDGE	Enhanced Data Rate for GSM Evolution
ESD	Electrostatic Discharge
EV-DOrA	Evolution Data Only Release A
GPIO	General-purpose I/O
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LGA	Land Grid Array

Acronym or Abbreviation	Expansion
LTE	Long Term Evolution
NC	Not Connected
PA	Power Amplifier
PCB	Printed Circuit Board
RF	Radio Frequency
RUIM	Removable User Identity Module
SMS	Short Message Service
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver-Transmitter
UL	Up Link
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
WCDMA	Wideband Code Division Multiple Access